

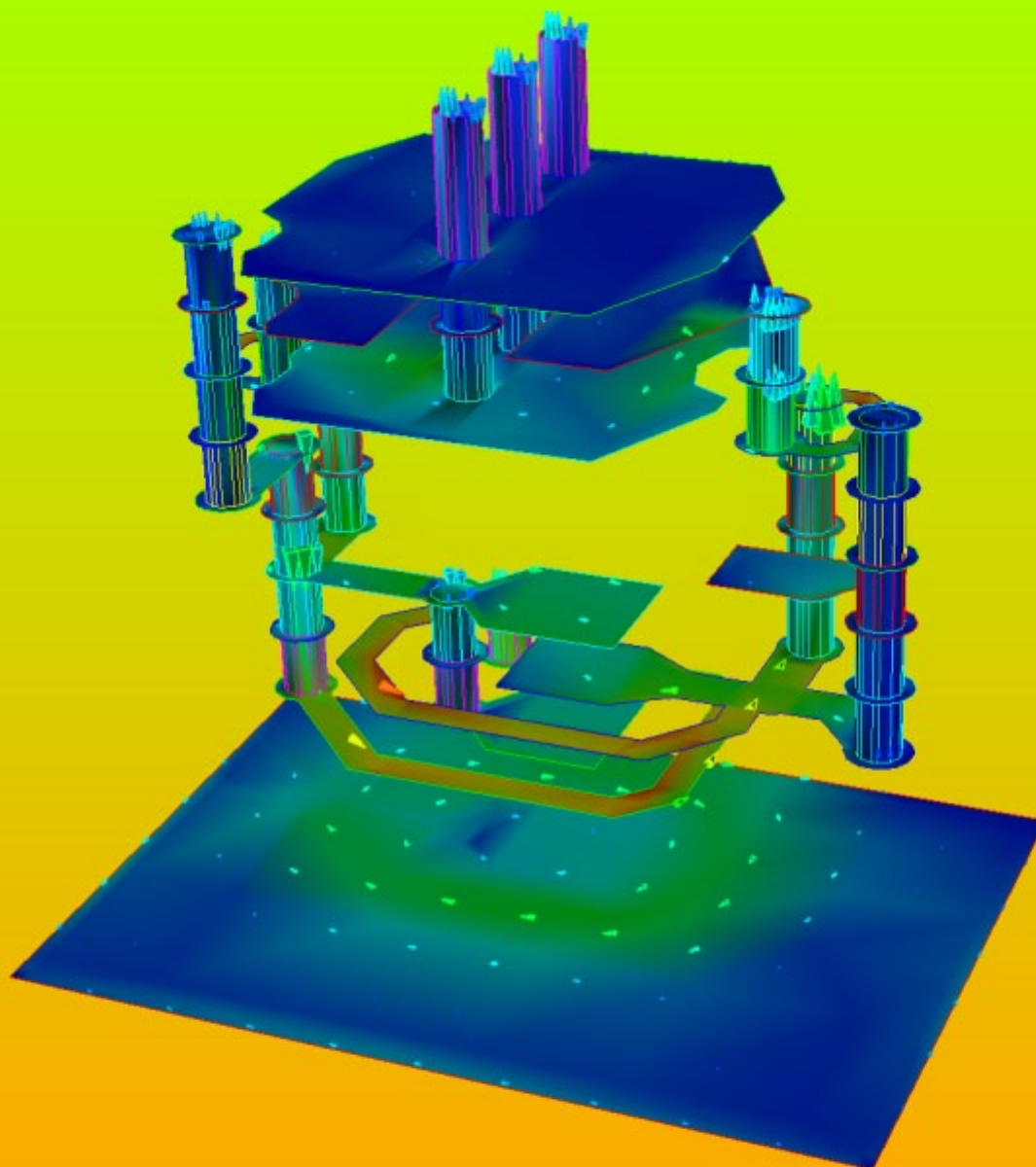
# EDN

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Issue 5

# europa



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***Top free DIY tools every engineer needs – page 14***

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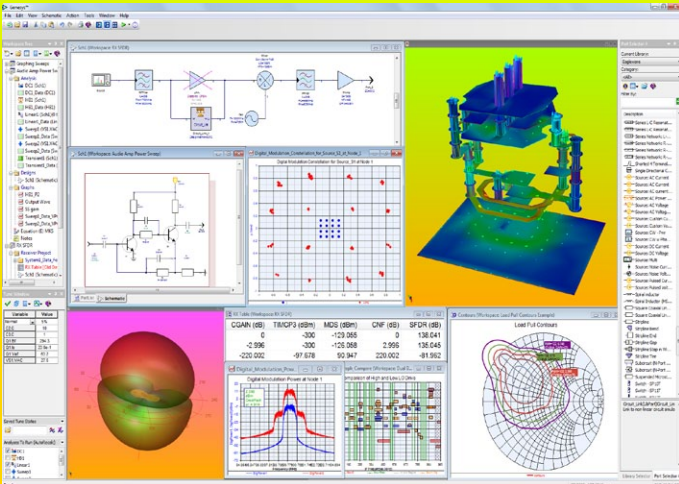
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## Cover image; Modulated RF analysis

The image on this month's cover is taken from a screen shot illustrating the capabilities of Agilent Technologies EEsof's Genesys EDA software, 2014 release. This release features modulated RF analysis as well as enhancements to its



custom-filter direct synthesis technology and, as depicted by the illustration, spans extraction from physical interconnect and layout, through to performance analysis of complete digital RF systems. Using Genesys 2014, designers can simulate digitally modulated RF

signals such as those found in today's defence and consumer wireless applications as easily as they do traditional analogue RF signals. The software delivers system budget analysis of these digital modulation metrics for every component in the system block diagram, all in a single pass. Underlying Genesys 2014's accurate digital modulation analysis is a new, embedded numeric dataflow simulator that also enables easy verification against the latest wireless standards for WLAN 802.11ac and LTE-3GPP. Click right for more details.



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# HEARTBLEED: THE WAKEUP CALL THE OPEN-SOURCE COMMUNITY NEEDED?

by Brian Dipert, writing for EDN

When the "Heartbleed" vulnerability in OpenSSL had just become public and looked as if it would have widespread effects, my immediate reaction was, "Heartbleed is big, bad, and recent enough that it justifies a column all its own." This is indeed that column. However, although I'll provide a brief background on Heartbleed's cause, effects, and in-progress fixes, plenty of other already-published literature already covers this same ground more extensively than I plan to. My particular angle on this topic is somewhat different, as you may already be able to tell from this post's title. If you need a refresh on SSL and OpenSSL, Wikipedia provides a suitable summary.

So what's Heartbleed? Wikipedia to the rescue again: "Heartbleed is a security bug in the open-source OpenSSL cryptography library, which is widely used to implement the Internet's Transport Layer Security (TLS) protocol. Heartbleed results from improper input validation (due to a missing bounds check) in the implementation of the Transport Layer Security (TLS) heartbeat extension, the heartbeat being behind the bug's name. This vulnerability is classified as a buffer over-read. The "heartbeat extension" is a critical piece of the puzzle. It's in effect an SSL-specific (and optional) implementation of the more general "ping" function, intended to enable a client system to discern that a server on the other end of the SSL connection is still present".

As an as-usual-excellent XKCD web comic concisely points out, the OpenSSL bug enables a heartbeat-initiating client to coax a server into engorging more information than intended. This information can potentially be nothing more than garbage ... or it could be registered users' account logins and passwords, for example. It was initially believed that private server RSA keys used to generate certificates might be safe, but that theory was unfortunately debunked quickly. And although the flaw has now been patched, the number of affected systems and software packages is vast, and they aren't necessarily easy to update (that is, if they ever get updated at all).

How did the OpenSSL mess happen in the first place? To understand the answer to this question, I'll first quote from a prior open source-themed post of mine, published in October 2012:

"Most open-source efforts are maintained by one or a handful of developers and 'supported' by a rag-tag band of enthusiasts, all of whom do so on the side by virtue of their (other) paying 'day jobs'."

You might think that OpenSSL, by virtue of its ubiquity, would be a well-funded exception to this rule. You'd think wrong (although the funding situation thankfully seems to be changing). As it turns out, Stephen Henson was the only full-time OpenSSL developer, and he's by no means living in the lap of luxury. The flaw was actually created by one of a short list of part-time contributors, Robin Seggelmann, made it through Henson's review undetected, and survived in the code base for more than two years before being discovered.

Open-source software has some compelling selling points. For one thing, it's free, and the many thousands of developer eyeballs

peering over it generally result in robust code.

So what about all those eyeballs, developer and implementer alike? Why didn't they catch it? Back to the BuzzFeed writeup I mentioned earlier for the explanation:

"This stems in part from how its current funding structure affects its priorities: For now, OpenSSL's development lives and dies by the OSF's commercial income, almost all of which comes from putting in new features, rather than maintaining the old. The current setup means, [OpenSSL foundation organiser] Steve Marquess readily admits, that "the fundamentals of OpenSSL are being neglected. No one is hiring us to maintain the current code base." And of course mistakes can happen. When they do, there currently isn't the money to pay a person, never mind a team, to go through the 456,332 lines of [C] source code with a fine-tooth comb to find them.

There are plenty of people looking at the OpenSSL code, including Professor Paterson, whose Information Security Group (ISG) at Royal Holloway is incentivised by the University of London to conduct research into OpenSSL and to spot bugs. But Paterson points out that there are significantly fewer people writing the code within the OpenSSL project than those on the outside looking in, scanning it for weaknesses — and the former are adding more stuff in, not taking stuff out and cleaning up the contradictions contained within the code base. The code has tripled in size from late 1998 and early 1999 when SSLeay became OpenSSL; on average 1,575 new lines of code have been added each month for the past 15 years.

And of course, among those thousands of eyeballs are sets with more nefarious objectives in mind, and access to source code enables them to develop exploits for unpatched, easily identified software builds.

This situation leaves me with an unanswered question that I've long pondered (and that others are now asking, as well); is open source fundamentally better than closed source? A closed-source equivalent to OpenSSL very well might exhibit the same Achilles Heel, but keep in mind that this bug wasn't discovered by source code perusal but by usage experimentation, which resulted in no fundamental benefit for open versus closed source. The ability to analyse open source code to identify and fix bugs is counterbalanced by the opportunity to exploit them, particularly when vulnerabilities are revealed before fixes are even in place. And although some folks object to the "monopoly" supply of closed-source code, OpenSSL highlights that open source software is no less single-sourced in many cases.

In March 2007 I wrote the following, which is eerily prescient in light of the Heartbleed situation:

"Open source or closed source? I really don't care, particularly if the manufacturer has used open source as a means of bolstering its profit margin versus enabling it to lower the product price versus a closed source alternative. And if the closed source product is more maintainable (assuming, of course, that the product is inherently vulnerable to potential code flaws .... a fair bet in this increasingly network-connected world of technology), I'll vote for closed source with my wallet."

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# pulse

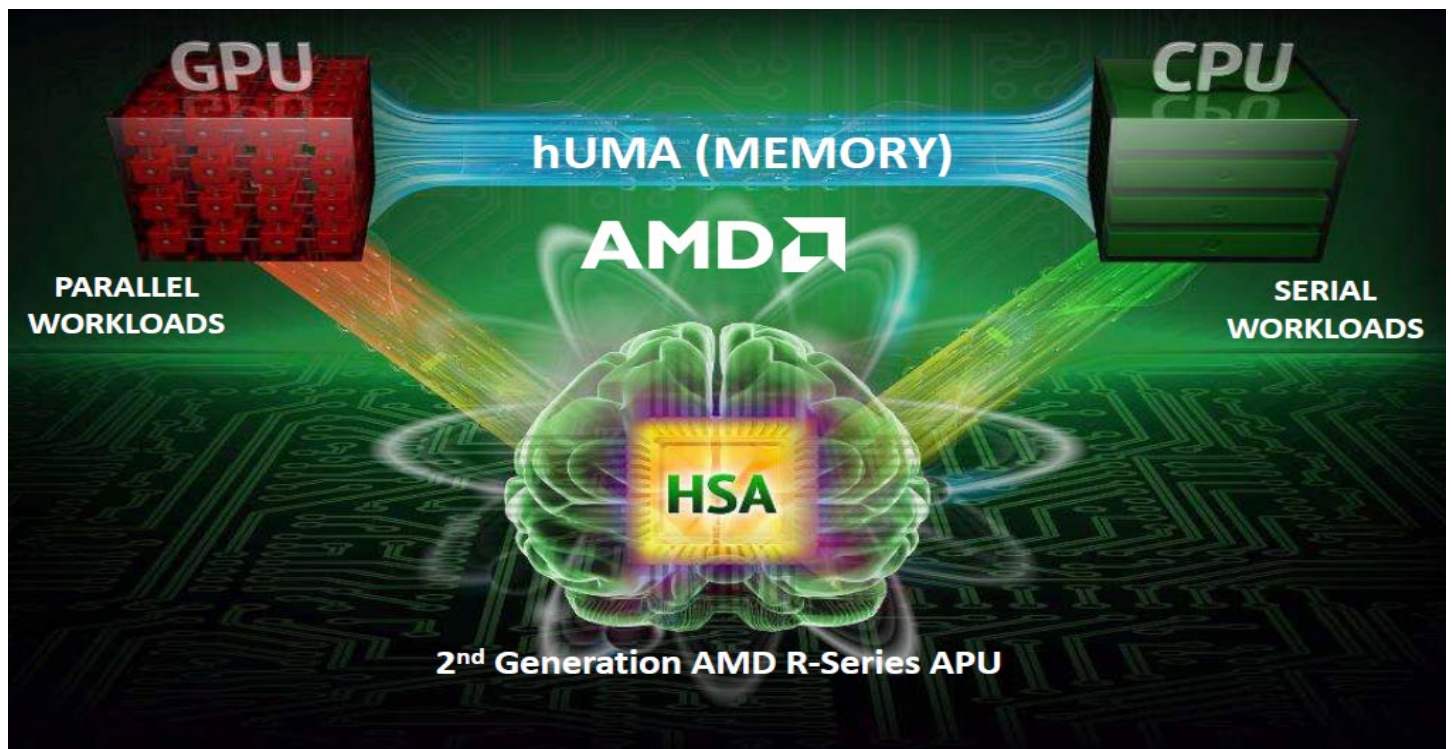
## AMD renews R series embedded APUs with HSA designs

**A**MD has introduced a second generation of its “R” series APU (combined CPU and graphics processing unit) for the embedded market, in 28-nm technology and with an implementation of the HSA (heterogeneous system architecture) to increase processing throughput.

The HSA aims to “unlock the GPU for embedded computing”. The many-core structure of the GPU has been available to embedded designers for some time, using the “GPGPU” approach – general purpose [computing using] the GPU. Previously, the GPU operated as a slave to the CPU, with tasks – that the programmer identified as having parallel attributes – for the

ingly and that while knowledge of, for example, OpenCL will continue to be useful in programming the chips, the objective is to open up the power of the product range to design teams that are not heavily graphics-oriented. “Think serial/parallel rather than CPU/graphics,” he added, also noting that there are many networking tasks that exhibit a high degree of parallelism. You will be able to include C++ code in a mixed-compilation flow and create a parallel implementation.

The second generation embedded R-series Accelerated Processing Unit (APU) (codenamed “Bald Eagle”) has multiple (up to four) x86 cores plus GPU; it supports 4k graphics and up to



GPU queued for it by the CPU, and each has its own memory space. In the HSA implementation the two cores have equal status, and can work together in a shared memory space. “Multiple compute tasks can work on the same coherent memory regions, utilizing barriers and atomic memory operations as needed to maintain data synchronization (just as multi-core CPUs do today),” – as AMD puts it. The program flow can move tasks – parallel or serial – to the most appropriate processing element, and the task does not have to move from memory space to memory space.

Asked about the implications for programming, an AMD spokesman said that code tool support will be updated accord-

four separate displays. Alongside AMD’s “Steamroller” CPU architecture is the AMD Radeon HD 9000-series GPU architecture that supports Microsoft DirectX 11.1, OpenGL 4.2 and OpenCL all within a 35W power envelope. (35W is for the quad-core version; a dual-x86-core device will have a 17W power envelope.)

The second generation embedded R-series APUs support Microsoft Windows and Linux, with Microsoft DirectX 11.1 and OpenGL 4.3 supported, along with OpenCL, giving developers access to computation power of the Radeon HD 9000-series GPU. This means whether applications run on Windows or Linux, R-series APUs will run them.



## 100V, normally-off, GaN transistors in low inductance, thermally-efficient packaging

**G**aN Systems has announced a family of normally-off 100V gallium nitride – GaN – transistors that spans 20-80A with very low on-resistance and total gate charge. The company contends that GaN represents such a step change in electrical performance that conventional package formats negate the benefits, and has designed its own easy-to-mount package format that has extremely low resistance and inductance.

GS61002P, GS61004P, GS61006P and GS61008P are respectively 20A/21 mΩ, 40A/11 mΩ, 60A/8 mΩ and 80A/5 mΩ parts while GS71008P is an 80A/5 mΩ half bridge device. These enhancement mode parts feature a reverse current capability, source-sense for optimal high speed design and exceptionally low Total Gate Charge ( $Q_g$ ) and Reverse Recovery Charge ( $Q_{RR}$ ). RoHS compliant, the devices are delivered in GaN Systems' near chip-scale, embedded GaNPX package which minimises inductance and optimises thermal performance. GaN Systems' Island Technology addresses cost, performance,

and manufacturability challenges of gallium nitride resulting in devices that are smaller and more efficient than traditional design approaches; larger devices are built with multiple isolated "island" transistor elements, and redundancy allows the company to overcome some inherent limitations of working in the GaN material. The package it employs on these transistors uses a built-up layer structure of conventional PCB material, with multiple vias providing a very short and low-inductance path from the top of the die back to the pads of the package.



Girvan Patterson, President of GaN Systems comments that to view a GaN transistor as a silicon replacement with a better parameter set is to miss the point; the electrical performance at device level can be so much better that a complete new design approach is needed to get the most out of the devices – and that all of the elements of such an approach are now in place.



**Honeywell**



Magnetoresistive Sensor ICs,  
Nanopower Series

**High sensitivity.**  
**Extremely low power.**

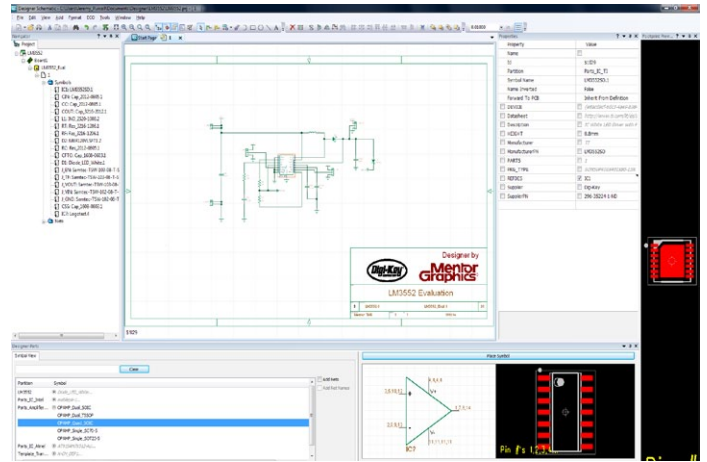


## Low-cost web-based EDA/PCB software from Mentor & Digi-Key

**D**istributor Digi-Key, and Mentor Graphics, have configured a design tool, described as “concept-to-prototype”, aimed at individual designers and intended to support “green-field” projects before transition to production. A Beta version of the package, which will be priced below \$300, is now available from Digi-Key.

Designer Schematic addresses (the two companies say) escalating demand from professional engineers for EDA software at an affordable price point for new R&D projects, while facilitating access to the latest parts. “Innovators ... need to have access to professional-class PCB design tools to easily capture their design concepts. Mentor Graphics’ partnership with Digi-Key provides an opportunity to deliver our proven design technologies to individual engineers at very attractive price points,” said Henry Potts, vice president and general manager of Mentor Graphics Systems Design Division, adding, “... Mentor Graphics is extending its range of PCB development solutions [to serve] individual engineers working on conceptual projects, [in addition to] the desktop market with PADS, and the extended enterprise with Xpedition.”

The Designer Schematic tool is scheduled to launch early this



summer, at a sub-\$300 price point. Engineers will access first-class design tools, and use new components with error-free EDA representation, as they are released, providing direct paths to quick-turn PCB layout and manufacturing services. The web-based software is designed to give engineers real-time access to the latest design components along with easy, error-free access to Design Service Providers and PCB Fabrication and Manufacturing Services.



## Integrated, nanopower magnetoresistive sensors offer new detection options

**H**oneywell has introduced a nanopower anisotropic magnetoresistive sensor IC; the technology provides position detection based on magnetic field sensing, using a very small and low-cost package, with on-chip integration of level detection and switching to give a simple on/off output and to replace reed switches where they are still the only option.

The device's high sensitivity, Honeywell says, allows you to cut costs, and to use the sensors in battery operated equipment with extremely low power requirements, where the solid state, non-contact design provides a reliable, durable alternative to reed switches.

The Nanopower Anisotropic Magnetoresistive Sensor ICs provide the highest level of magnetic sensitivity (as low as 7 Gauss typical) while requiring nanopower (360 nA average, in a typical reed-switch-replacement application). Smaller and more durable and reliable than reed



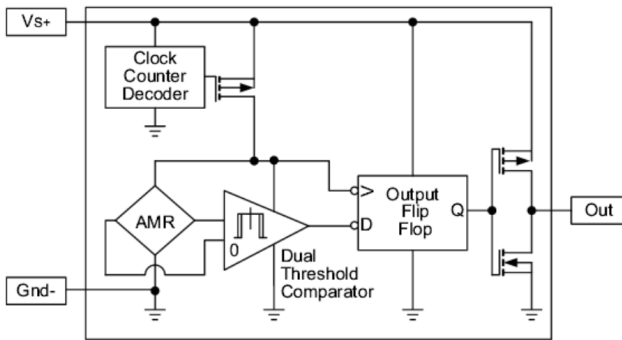
switches, at the same sensitivity and essentially the same cost, the new sensor ICs can be deployed where previously only reed switches could be used for reasons of low power requirements and large air gap needs. The 360 nA figure is based on a 0.015% duty cycle of typically 15 µsec wake/100 msec sleep cycle.

Response time is not specified in the initial data sheet; the 100 msec cycle appears chosen to match the requirements of a typical reed-switch application, detecting whether or not (say) a door is open or closed, within 1/10th of a second. The 15 µsec on-time implies an actual detection in single-figures-µsecs, which could support detection of events at up to (perhaps) around 100 kHz – at the cost of running the device at its on-state current, which is 1 mA typical – sleep current is 160 to 260 nA over the supply voltage range.

These ICs’ higher sensitivity can function over air gaps twice the distance that Hall-effect sensors can accommodate. The higher sensitivity improves design flexibility and can offer significant application cost savings by utilising smaller or lower strength magnets.

“Due to the significant price increases for rare earth magnets, design engineers using Hall-effect sensors have been looking for ways to decrease the total cost of design by using less magnetic material, or moving to a more common magnet in their applications,” said Josh Edberg, senior product marketing





manager for Honeywell Sensing and Control. The Nanopower Series is available in two magnetic sensitivities: Ultra-high sensitivity SM351LT: 7 Gauss typical operate, 11 Gauss maximum operate, very low current draw (360 nA typical); Very high sensitivity SM353LT: 14 Gauss typical operate, 20 Gauss maximum operate, very low current draw (310 nA typical). The sensors operate from 1.65 to 5.5V.

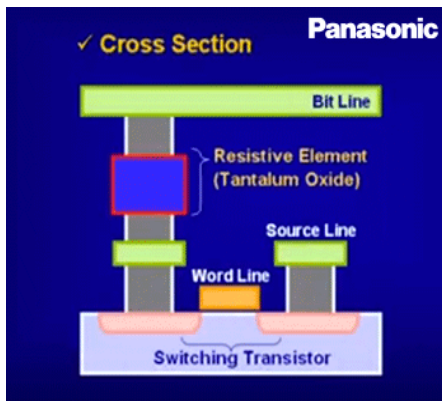
Complete article, here

## Panasonic's MCUs with resistive RAM, in distribution

Mouser Electronics has the MN101L 8-bit Microcontrollers from Panasonic, the first microcontrollers with internal Resistive RAM (ReRAM). Resistive RAM is a new non-volatile embedded memory that offers five times the write performance of Flash or EEPROM memory without the need for an erase cycle. This has the benefit of offering high-speed non-volatile writing and longer operational times in battery powered devices.

Panasonic's Resistive RAM is based on a cell structure where a binary "1" and "0" is read based on the resistance of a thin-film metal oxide (tantalum oxide) sandwiched between two electrodes on the top and bottom of the metal oxide. The state of the memory cell is changed to a "1" by applying a pulsed negative voltage to the top electrode. This causes oxygen ions to migrate into the tantalum oxide, lowering the resistance and making the cell conductive to electricity. The state of the cell is changed to a "0" by applying a pulsed positive voltage to the top electrode. This causes oxygen ions to migrate away from the tantalum oxide, raising the resistance and making the cell non-conductive. The simple structure of a

metal oxide stacked vertically between two electrodes results in excellent low power consumption and high-speed rewriting characteristics.



These Panasonic 8-bit MCUs have a total of 64 kBytes of ReRAM. 62 kBytes is used in the program memory area and is used in a similar way to conventional Flash memory. 2 kBytes of ReRAM is used in the data memory area and is used in a similar manner to EEPROM. ReRAM requires a write voltage of only 1.8V. Program Memory ReRAM has an endurance of 1K write cycles while ReRAM used as data memory is rated at up to 100K write cycles. Data retention is 10 years.

The Panasonic MN101L uses a simple 10 MHz 8-bit MCU core with a three-stage pipeline. It includes a 16x16 multiply, 32/16 divide, Real Time Clock (RTC), ADC, and an LCD controller. The Panasonic MN101L Series Evaluation Board, also available from Mouser Electronics, helps developers evaluate the MN101L and test Panasonic's new ReRAM technology.

Complete article, here

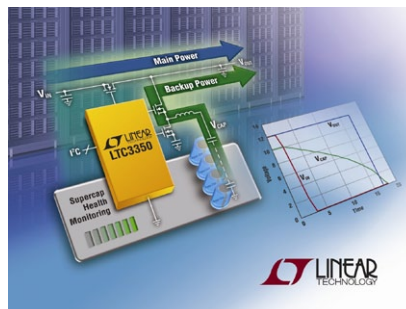
## 10-A backup power controller manages supercapacitor stacks

LTC3350 is a supercapacitor charger and backup controller IC that includes all of the features necessary to provide a complete, standalone capacitor-based backup power solution to provide short-term uninterrupted power in the event of a main power failure, for data backup for solid state drives (SSDs) and nonvolatile dual in-line memory modules (NVDIMMs), power fail alarms in medical and industrial applications, as well as a host of other "dying gasp" power fail indicators.

LTC3350 provides all PowerPath control, capacitor stack charging and balancing, and capacitor "health" monitoring to ensure that the backup system is capable of reliable operation. It features a wide 4.5V to 35V input voltage range and over 10A of charge/backup current capability. The device also provides balancing and overvoltage protection for a series stack of one to four supercapacitors. The LTC3350's synchronous step-down controller drives N-channel MOSFETs for constant current/voltage charging of the capacitor stack at up to 5V per cell. In backup mode, the step-down converter runs in reverse

as a synchronous step-up DC/DC to deliver power from the supercapacitor stack to the system supply to be backed up.

The LTC3350 contains an accurate 14-bit analogue-to-digital converter (ADC), which continuously monitors input and output voltage and current. In addition, the internal measurement system monitors parameters associated with the backup capacitors themselves, including capacitor stack voltage, capacitance and stack ESR (equivalent series resistance) to ensure adequate energy storage and power delivery during backup. By monitoring the actual capacitance of the backup supercapacitors, the LTC3350 provides longer capacitor life by enabling the system to set the capacitor voltage to a minimum value while ensuring the required backup energy is maintained. All system parameters and fault status can be monitored



via a two-wire I<sup>2</sup>C interface, and alarm levels can be set to alert the system to a sudden change in any of these measured parameters.

Complete article, here

# Reference design outputs 4 analogue variables, cuts component count

Using one-third fewer components, this high-efficiency reference design from Maxim Integrated, the Alameda subsystem, is a flexible 4-channel bipolar analogue output module for industrial automation applications.

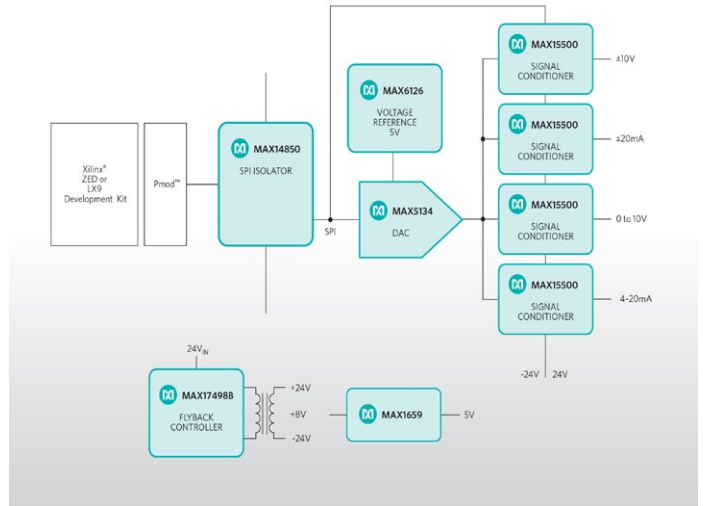
You can add a high-accuracy, 4-channel analogue output to an industrial automation designs with 33% fewer components than competitive designs, Maxim says; industrial programmable logic controllers (PLCs) need multiple, flexible, high accuracy analogue outputs. The Alameda subsystem combines four high-accuracy ( $< \pm 0.1\%$ ) outputs with a high-efficiency, low-noise power supply controller on a single board. Alameda offers great flexibility—its outputs are configurable to  $\pm 10V$ ,  $\pm 20\text{ mA}$ ,  $0$  to  $10V$ , or  $4$ – $20\text{ mA}$  for current and voltage applications. Automatic error reporting for detecting open and short circuits, brown-outs, and over-temperature conditions make this subsystem ideal for demanding, precision industrial control and automation applications.

### The design...

- is fully tested: schematics, layout files, and firmware are available for immediate use and customisation.
- uses fewer components: unique, integrated parts reduce number of components by 33% compared to competitive designs.
- speeds designs: integrates an efficient power supply with a 4-channel analogue output in a single compact system to solve noise issues and save engineers development time.
- improves PLC system reliability: automatically detects short-circuit, open-circuit, brown-out, and over-temperature conditions.

A second Reference Design from Maxim is aimed at gathering electricity distribution data faster and more accurately. The Petaluma reference design enables more intelligent grid data

Alameda Reference Design: 4-Channel Analog Output  
MAXREFDES24#



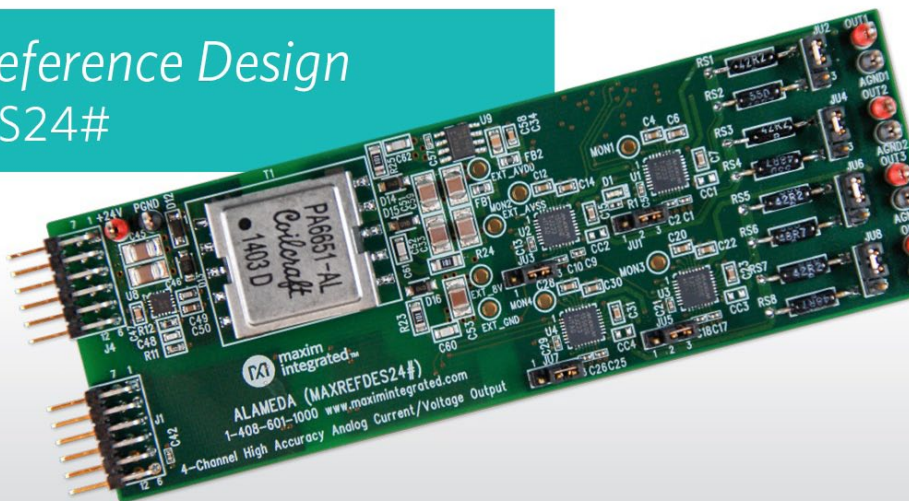
management with 3-phase, high-speed analogue data collection, yielding real-time measurements for utilities and infrastructure providers to simultaneously and accurately measure distributed power grid data.

Utility organisations worldwide, says Maxim, are deploying more robust applications that require highly accurate distributed grid status data to exploit distributed generation technologies such as solar and wind power. Voltage and current measurements must be gathered simultaneously for all lines, so the utility can understand the timing among phases and ensure maximum up-time across the grid. Petaluma is a high-speed, simultaneous-sampling, 8-channel analogue input front-end (AFE) that monitors grid data simultaneously from all phases, so grid managers

can optimise their distribution automation signal chain.

Petaluma is tuned to the 50 Hz to 60 Hz signal to match power grids around the world. The simultaneous sampling of three phases is done with low power consumption in the 1W range. Its high-speed sample rate (250 ksamples/sec per channel) comes with 16-bit accuracy, allowing for quick responses to grid fault conditions.

## Alameda Reference Design MAXREFDES24#



Complete article, here

# 14-bit, 2 Gsample/sec converters boost performance, ease of use

Analog Devices has introduced two high speed analogue-to-digital converters at 14-bits and 1 or 2 Gsamples/sec, that the company says are the best such parts for handling wide bandwidth signals, with wide dynamic range, while providing the linearity required for undersampling.

The parts feature a range of integrated functions to help you exploit their performance, and to simplify their use; the “break-through performance, bandwidth, and integrated functionality” will drive applications further towards direct-RF sampling, ADI asserts.

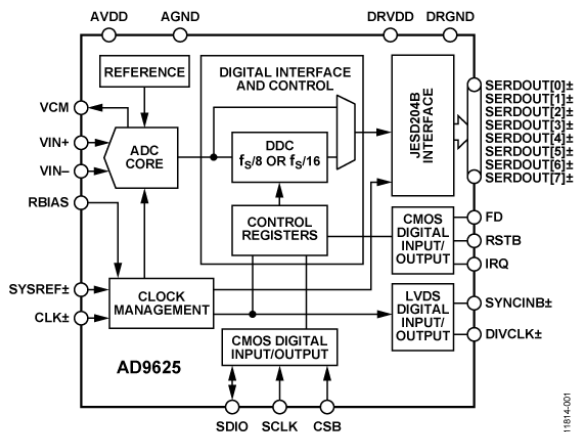
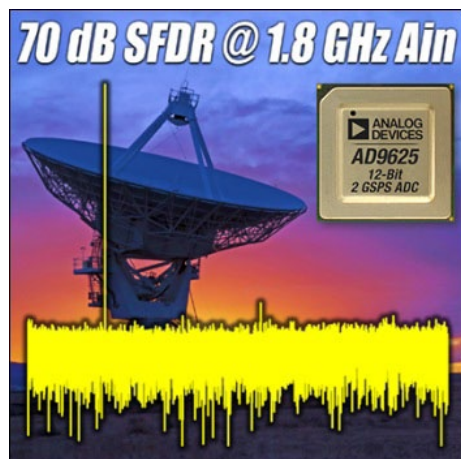
AD9680 is a dual-channel, 1.25-V, 14-bit, 1-Gsample/sec A/D converter featuring the best noise and dynamic range performance in its class enabling the trend for direct RF sampling in communications, instrumentation and military/aerospace applications. Its noise density of -154 dBFS/Hz is the lowest in the industry. Wideband RF data acquisition allows for better signal extraction in congested RF environments, over a wider bandwidth; the device also features four digital down-converters to assist with isolating a specified fraction or subset of the overall bandwidth. The AD9680 is interoperable with FPGAs from major manufacturers and supported with known good configurations, and offers ease of interfacing.

The AD9680, ADI says, allows more degrees of freedom for system designers trading off signal bandwidth, noise and linearity because it can digitise a DC to 2-GHz input signal with an accompanying dynamic range performance that was previously unavailable on the open market. You can increase signal sensitivity and bandwidth data rate, while enabling the use of an advanced reconfigurable data acquisition or radio platform. The A/D converter is available with an evaluation board design environment and reference designs for rapid system prototyping and board-level design and layout.

The AD9680 was designed for sampling wide bandwidth analogue signals up to 2 GHz with best-available dynamic range and noise performance over its rated bandwidth range. When converting a 1-GHz input, the converter achieves spurious-free dynamic range (SFDR) performance of 80-dBc and 61.5-dBFS signal-to-noise ratio (SNR) while consuming 1.65 W of total

power per channel. 2-Gsample/sec data converter

Also announced by ADI is the AD9625 that, “combines high bandwidth with industry-leading dynamic range and noise for first time in a 2-GSPS data converter to drive applications to direct RF sampling.”



This part is a 12-bit, 2-Gsample/sec, AD9625 A/D converter. It provides the best noise and dynamic range performance in its class for better receiver sensitivity along with the ability to discern smaller signals in the presence of noise, clutter, blockers and interferers. This performance combined with 2-Gsample/sec bandwidth and integrated signal processing functionality enables the trend to direct RF sampling in communications, instrumentation and military/aerospace applications. The converter’s noise spectral density of 149.5 dBFS/Hz, coupled with high-input bandwidth, allow designers to use undersampling system architectures into the 2nd Nyquist zone, saving on a frequency down-conversion stage.

An ADI spokesman confirmed that the 9265 – a single channel part – is not a variant of the 9680, interleaving the two channels of the 9680, but is a completely separate design. It shares features with the 9680, in that it also has additional on-chip functionality for ease-of-use, such as digital-down-conversion to select a subset of the input bandwidth; and the JEDEC JESD204B interfacing capability.

The AD9625’s wider input bandwidth enables advanced RF sampling architectures and allows designers to reduce the number of analogue frequency down-conversion stages and their associated noise and cost contributions. The simplified system architecture eliminates the need to interleave multiple A/D converters to obtain needed performance and allows for development of reconfigurable platforms. It is available with an evaluation board design environment and reference designs to simplify system prototyping and board-level design and layout.

The AD9625 achieves 80-dBc spurious-free dynamic range (SFDR) with a 1-GHz input. The AD9625 is, ADI claims, the only open-market-available 12-bit, 2-Gsample/sec, A/D converter that simplifies the digital interfacing challenge by integrating two digital-down converters (DDC), two numerically controlled oscillators (NCO) and a configurable JESD204B serial link for the output data.

Key applications include ultra-wideband RADAR, wideband front-ends for digital storage oscilloscopes and data acquisition platforms.



# HYBRID EXECUTION - THE NEXT STEP IN THE EVOLUTION OF HARDWARE-SOFTWARE CO-DEVELOPMENT

Software has become a crucial component as it determines significant portions of the functionality visible to end consumers, as well as differentiation.

Over the past decade the software content to be addressed by semiconductor companies has multiplied several-fold. Where providing some core drivers and managing an ecosystem of operating system (OS) providers was sufficient in the late 90's to win a socket in the mobile space, today the contenders for providing an application processor have to be able to deliver the chip with multiple OSs already ported, up and running, ready to be adopted by system customers.

Unfortunately, in classic development flows, hardware and software – while ultimately derived from joint requirements – diverge in their development and in the worst case integration doesn't happen until a “big-bang” integration test is done.

The upper portion of Figure 1 shows such a disconnected hardware-software development flow from requirements through preliminary design, unit coding, testing and integration. The system integration at the very end often brings surprises that cannot be overcome without significant re-development. The industry has been striving for years to achieve a fully agile system development flow as indicated in the lower portion of Figure 1. Integration ideally should happen early and then be repeated often.

Given its importance, software has become the long tail in development cycles and its efficient development and testing is of great concern. Design teams are attempting to develop software as early as possible on whatever representation of the hardware they can get their hands on – achieving what the industry sometimes calls the great shift to the left. In an ideal world software development would be enabled at the very start of a chip-development project, but in reality users face various development options across levels of abstraction and different execution engines.

Hardware execution engines to enable early software development;

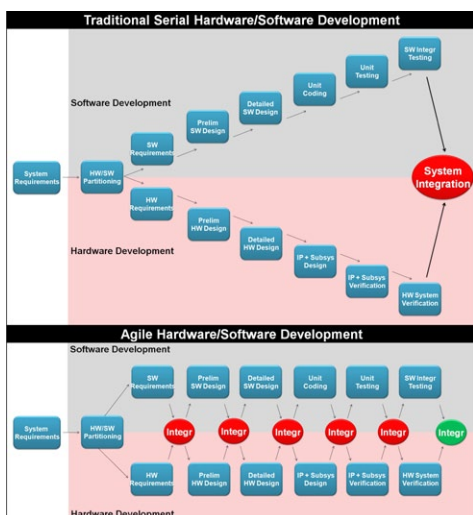


Figure 1. The need for an agile hardware/software development flow.

Figure 2 illustrates the situation, outlining the various development engines that project teams consider using to bring hardware and software together as early as possible.

During a chip development project, verification and software development is mainly done on four different core execution engines.



Figure 2. There is no one-fits-all solution.

## Virtual prototypes

Virtual prototypes are transaction-level representations of the hardware, able to execute the same code that will be loaded on the actual hardware, and often executing at well above 100 MIPS on x86-based hosts running Windows or Linux. To the software developer, virtual prototypes look just like the hardware because the registers are represented correctly, while functionality is accurate but abstracted. As an example, processor pipelines and bus arbitrations are not represented with full accuracy. While they can be made available to users early in the design flow, one of the challenges project teams need to consider is that modelling may take time and effort for which the return on investment (ROI) has to be considered carefully. Especially for designs that contain a large percentage of IP-reuse, remodelling of existing RTL may be a non-feasible hurdle to take in cases for which an IP provider does not provide transaction-level models for the licensed IP. In addition, even if transaction-level models have been developed, keeping them synchronised with the actual implementation as it is undergoing changes, requires effort that often is not invested and leads to a situation that the initial models are no longer synchronised with the final implementation. As a result, for smaller designs virtual prototypes may not even be considered by project teams.

## RTL simulation

Register transfer level (RTL) simulation executes the same hardware representation that is later fed into logic synthesis and implementation. This is the main vehicle for hardware verification and it executes in the Hertz range, but it is fully accurate as the RTL becomes the golden model for implementation, allowing detailed debug of the hardware. However, its limitations in speed make it infeasible for larger scale software development such as operating system (OS) bring-up. If at all used for software development, users will do smaller scale software development for drivers and lower layers of the software stack. Due to RTL being the “golden” description from which the implementation can be automatically derived using logic synthesis, RTL simulation is the minimum that project teams require for verification of the hardware.

The author continues with an outline of the alternative approaches of Emulation and FPGA prototyping, before looking at the solutions that are emerging as “sweet spot” options for today's designs, and at progress towards an Agile hardware/software development environment. Click right.





# Analog Tips

## SIMPLE RC NETWORK REDUCES LDO NOISE BY GLENN MORITA

Noise is extremely important to designers of high-performance analogue circuits, especially high-speed clocks, analogue-to-digital converters, digital-to-analogue converters, voltage-controlled oscillators, and phase-locked loops. A low-dropout regulator (LDO) can power these circuits. A key to reducing LDO noise is keeping its noise gain close to unity.

The figure shows a simplified block diagram of a typical adjustable-output LDO. The output voltage,  $V_{OUT}$ , is the product of the reference voltage and the DC closed-loop gain of the error amplifier:  $V_{OUT} = V_R \times (1+R1/R2)$ , where  $(1+R1/R2)$  is the DC closed-loop gain of the error amplifier. The noise gain is equal to the DC closed-loop gain. Reducing the noise gain can reduce the output noise of adjustable-output LDOs where the feedback node is accessible.

Adding a simple RC network reduces the output noise while improving the power supply rejection and load transient response. The network formed by R3 and C1 reduces the AC gain of the error amplifier. To ensure stability with LDOs that have low phase margin or are not unity-gain stable, choose R3 to set the amplifier's high-frequency gain to approximately 1.1. To reduce noise in the 1/f region, choose C1 to set the low-frequency zero to less than 10 Hz. With the noise-reduction network, the AC gain is close to unity for much of the bandwidth, so the reference noise and error amplifier noise are amplified to a lesser degree.

With this network, the noise performance shows significant improvement between 20 Hz and 2 kHz. Above the zero created by R1 and C1, the noise characteristic with the noise-reduction network is nearly the same as it is at unity gain. Above 20 kHz, the closed-loop gain of the error amplifier meets the open-loop gain, so no further reduction in noise gain is possible.

The power supply rejection ratio (PSRR) over this frequency range also improves. The amount of improvement, in dB, is approximately  $20 \times \log(1+R1/R3)$  for frequencies below where the closed-loop gain and open-loop gain converge. The overall PSRR increases by about 17 dB from 100 Hz to 1 kHz. The improvement decreases until about 20 kHz where the open-loop gain and closed-loop gain converge.

The noise-reduction network also improves the LDO's transient load response. With the noise-reduction network, the LDO is able to respond to the load transient in less than 50  $\mu$ sec, as compared to 500  $\mu$ sec without the network.

One drawback to the noise-reduction network is that it increases the startup time, from about 600  $\mu$ sec to 6 msec with  $C1 = 10$  nF and 600 msec with  $C1 = 1$   $\mu$ F. This should not be an issue

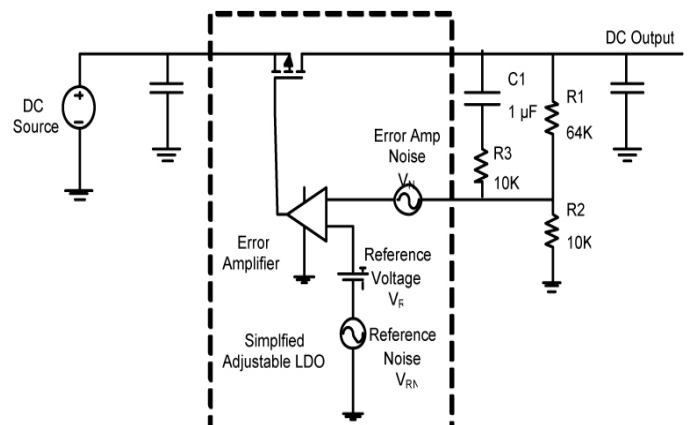


Figure 1. Simplified adjustable LDO block diagram shows internal noise sources.

for applications that do not switch the LDO off and on once the circuit is fully powered.

This technique will work with LDOs with architectures similar to that shown in the figure, where both the reference voltage noise and the error amplifier noise are amplified by the DC closed-loop gain. LDOs such as the ADP125, ADP171, ADP1741, ADP1753, ADP1755, ADP7102, ADP7104, and ADP7105 all share this general architecture and will benefit greatly from the use of a noise-reduction network.


Newer, ultralow-noise LDOs such as the ADM7151 will not benefit from the noise-reduction network because the architecture uses the LDO error amplifier in unity gain, so the reference voltage is equal to the output voltage. In addition, the internal reference filter has a pole below 1 Hz, heavily filtering the reference voltage and virtually eliminating any reference noise contribution.

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# TOP FREE DIY TOOLS EVERY ENGINEER NEEDS

Every electrical engineer who does DIY projects knows that dozens of free resistor calculators are out there that can save quite a bit of tedious work. Other simple tools can be found, but traditionally the free tool arsenal would stop there. Sure, there are base platforms such as SolidWorks and Autodesk, but what happens when they are missing a feature needed at that exact moment?

Now we're seeing a relative explosion in free tools for engineering electronics. It is easy just to hit the Net and use the myriad resources available. Some of those online tools prove to be worthless, and it's back to blind searching or some paid tool, but free software extends far beyond the functionality of a simple calculator.

To help sort out the nonsense from the useful online tools, check out the list in Figure 1.

## Calcuatoredge: when one calculator isn't enough

One of the more useful tools in an engineer's toolbox is a physical calculator. Why does it seem to get lost when it's truly needed? Workstations usually save the day. Those included in your OS of choice (Windows, iOS, Linux, etc.) are good for simple tasks but not so great for other things, even in scientific mode.

Searching for the right one online will net you roughly 131 million choices. Which one are you to choose when there are so many? Why not choose them all?

Almost all calculator versions known to humankind are located in one convenient site, **Calcuatoredge**. It boasts no fewer than a few hundred calculators for just about every field imaginable (and perhaps some that are unimaginable), including electrical, mechanical, civil, chemical, and even math. There's no need to search aimlessly for that obscure number cruncher ever again. Some of the more complex calculators even come with some rudimentary instructions.

## Cedar Logic Simulator on SourceForge

When it's time to test simple digital logic gates and registers or even some high-level components, you can turn to Cedar



Figure 1. Calculator choices from Calcuatoredge: this is only the "Electronic Engineering" panel.

Logic Simulator (still in beta edition), hosted on SourceForge, for some free online simulations. Designing circuits is great and all, but will they function correctly and perform when it counts? The Cedar Logic Simulator allows users to perform test simulations at the transistor, register/transfer, gate, and other levels.

The software also can be used as an introductory tool for teaching logic design and an entry platform for circuit design by allowing users to

drag and drop gates, inversions, and connections. There are also options for undo/redo and copy/paste functions. Projects can even be exported to monochrome or colour bitmap files for project integration.

SourceForge's main application window allows users to move back and forth through 10 different pages for multiple projects, making it one of the better free applications on the Web.

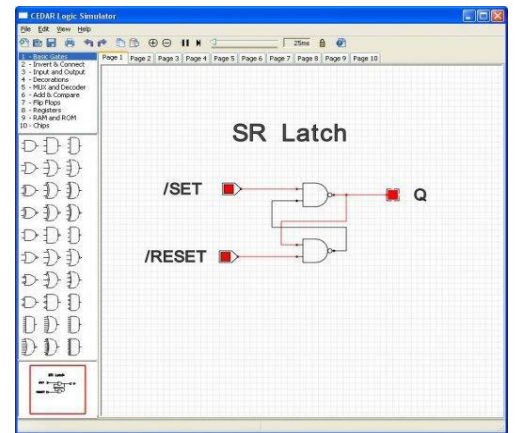


Figure 2. Cedar Logic Simulator, on SourceForge

## Logisim 2.7.0, an alternative to Cedar Logic Simulator

The Cedar Logic Simulator isn't the only free simulation tool available on the Internet. Tools that rival its design and simulation applications include Carl Burch's Logisim logic simulator. Students of the computer sciences often use the app as an introductory circuit design/learning tool, but it's practical for use outside the classroom, as well.

Logisim incorporates some of the same features as Cedar, including design and simulation platforms with preconfigured elements: AND, OR, NOT, etc. However, the software provides more in-depth functionality, including a tool for drawing colour-coded wiring connections that make programming and debugging a little easier. One of the more interesting aspects of Logisim is that it's portable and can be stored on removable storage media. It also can be used on any Windows-based PC, and it runs immediately after you click on the program. That's a luxury in today's install-but-with-malware world.

Click right for Carl's continuation of this article, in which he looks at circuit simulators, CAD packages for schematic capture, PCB layout, 2D and 3D design, and even free CNC machine control.

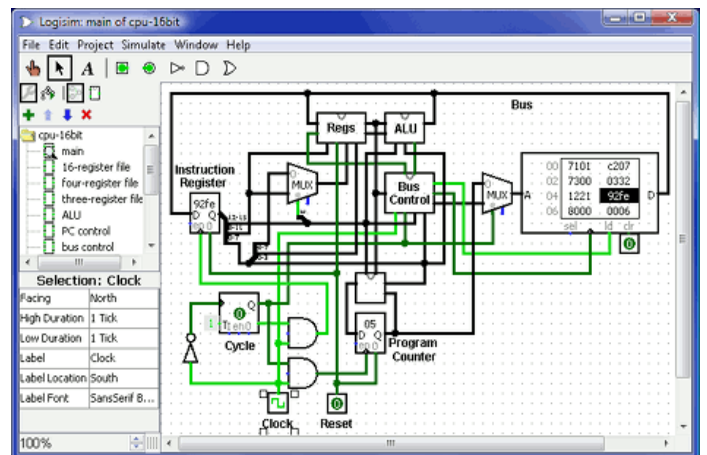


Figure 3. A screenshot from Logisim 2.7.0.

# UNDERSTANDING EFFICIENCY: LOOKING FOR THE WORST-CASE SCENARIO

It's standard practice to put the best-case scenario on data sheets, but how does that differ from the efficiency that can actually be achieved in your application?

Efficiency is one of the key parameters to consider when selecting the correct switch mode power supply. Pressure on equipment designer to deliver more functionality in a small size can result in more power being required which has a direct effect on the form factor of the power supply. The consequence of this is power supplies now have to deliver more output power in a smaller form factor. This, coupled with the need to meet more demanding environmental legislation and to minimise or eliminate fan cooling, is forcing equipment designers to look for more efficient power supplies.

An efficient power supply means less power is wasted as heat, which is the biggest factor in reliability of electronic components. Efficiency therefore has a big effect on the reliability and lifetime of the end equipment. Selecting an efficient power supply may also mean the equipment can be designed for operation without a cooling fan, reducing the audible noise, which is very desirable in many applications.

When deciding on a particular power supply for a piece of equipment, the minimum efficiency required for the equipment to run without a cooling fan, or with a certain lifetime guaranteed, may be calculated. The designer then turns to power supply data sheets to decide whether a particular supply meets those minimum efficiency criteria.

Equipment designers should be aware that the efficiency figure quoted on the manufacturer's website or data sheets is almost certainly a best-case scenario. The headline efficiency found on marketing material is true only when the power supply is run under favourable, or indeed, optimum, conditions. The actual conditions the power supply will experience be used in could be very different.

For example, it's common for the same model of industrial and medical equipment to be sold worldwide. Even if a power supply states it has a 'Universal Input', that doesn't guarantee its efficiency matches the headline efficiency for all inputs. The efficiency at the highest input voltage, European mains at 230 VAC, will be different to the efficiency the power supply can achieve at the lowest input voltage, Japanese mains at around 100 VAC or 115 VAC in North America.

The power supply's efficiency, when it's working under the most challenging set of operating conditions, may be thought of as the worst-case efficiency. This worst-case efficiency can be calculated by digging deep into the product's specification, which is essential to ensure the correct product is selected. A

product may be selected on headline efficiency alone, perhaps at an attractive cost level, only to find that at the worst-case operating conditions, a cooling fan is needed or a higher power output supply must be used deliver the performance required. Incorrect selection will result in increased cost, which is why it's vital to work with worst-case efficiencies from day one.

## Factors affecting efficiency

Efficiency is calculated as the output power divided by the input power, and is usually expressed as a percentage. The difference between the input power and output power is the power wasted in the power supply as heat.

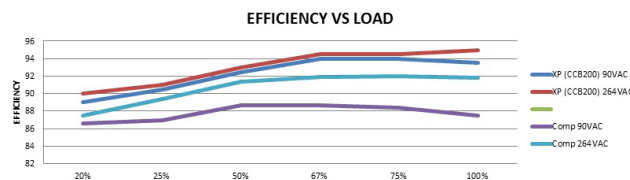
The input power is the product of the input voltage, current and power factor. If the input voltage (ie. mains voltage) is lower, to supply the same output power the current will have to increase, resulting in greater losses in the power components. The losses in the inductors and transformers are  $I^2R$ , where R is the resistance of the component. For the same efficiency, halving the input voltage results in twice the input current. In reality the input current is more than double due to the reduction in efficiency caused by increased power losses, resulting in more

than quadrupling the power loss of some of the components within the power supply and more than doubling the losses in others.

The same phenomenon exists for the output power, calculated as the product of the output current and output voltage. The optimum output voltage is the highest the PSU can supply; at lower output voltages, currents increase, and some losses increase proportional to the square of the current.

As an example, a comparison between the efficiency of the XP CCB200 at 264 and 90V, and that of a comparable AC-DC power supply from another manufacturer is shown in Figure 1. The different curves show the efficiency at the lowest possible input voltage (Japanese mains minus 10%), and the highest (UK mains plus 10%). With the two different input voltages, the efficiency of the XP CCB200 varies 1-2%, whereas the other power supply's efficiency drops almost 5 percentage points at full load when switching to the lowest input voltages. Putting this in terms of wasted power, the XP product would dissipate 2W to 4W more power at the lower input voltage, whereas the power supply from the other manufacturer would dissipate nearly 10W more power. This device's headline efficiency is 92%, but by switching to Japanese/North American voltages, the maximum efficiency it can achieve is 88.5%, and then only under specific load conditions.

*In the continuation of this article, the author notes the effects on efficiency of additional parameters, and of power supply topology – click here.*



**Figure 1-** Power supply efficiency over variable load conditions, with different supply voltages. Curves for the XP CCB200 and a comparable supply from another manufacturer are shown.



# BANDPASS FILTER, ADJUSTABLE Q, CONSTANT MAXIMUM GAIN WITH TWO OP-AMPS

**B**andpass filters (BPF) are widely used for very narrow frequency bands with attenuation of any range of frequencies.

Equation (1) expresses the second-order bandpass transfer function of a BPF:

$$H_{BP}(s) = K \frac{\frac{s}{\omega_0}}{\left(\frac{s}{\omega_0}\right)^2 + \frac{1}{Q}\left(\frac{s}{\omega_0}\right) + 1} \quad (1)$$

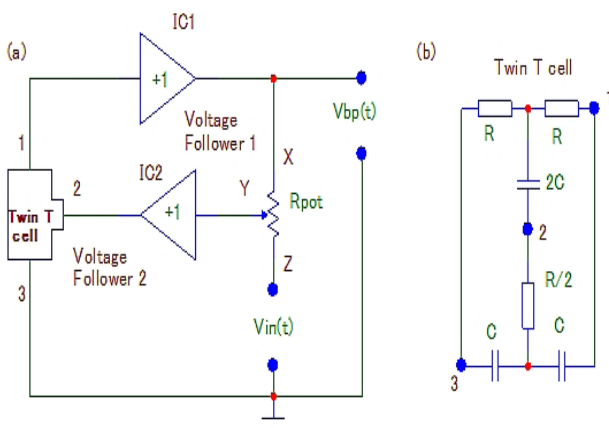
Where K represents constant filter's gain, Q represents the filter's quality factor.

In article by H. Martínez et al. (Ref. [1]) they describe a BPF with adjustable quality factor and constant transfer coefficient at the resonant frequency designed with three op-amps. The transfer function of this BPF corresponds to expression (1), in which K is inversely proportional to quality factor Q. This bandpass filter with an adjustable quality factor (Reference 1, Figure 1) comprises a twin T cell and a differential stage.

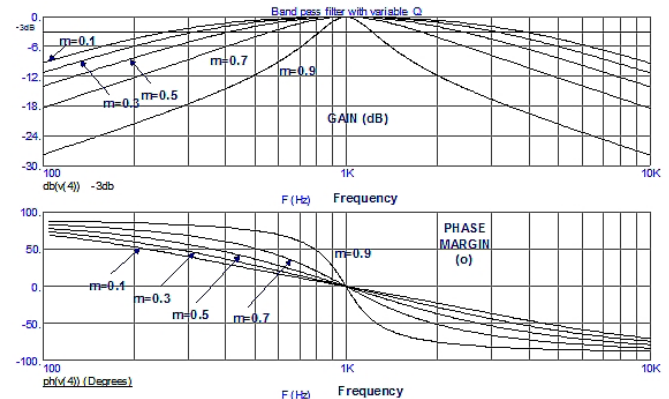
This design discussed here allows us to exclude the differential stage from the scheme of BPF. Properties of the scheme offered by H. Martínez et al. all remain.

The block diagram of the BPF shown in Figure 1a, shows a voltage-follower using IC1 and IC2, may be implemented using a standard dual operational amplifier by connecting its inverting inputs to the op-amp outputs.

The BPF (Figure 1) is based on a Twin-T configuration (Figure 1b).



**Figure 1-** Scheme of active BPF (a) provides a change in quality factor, while maintaining constancy of the gain coefficient at a resonant frequency based on twin T cell (b) The Twin T cell without the differential amplifier.



**Figure 2-** Magnitude and phase Bode plots at the BPF output,  $V_{OUT}(t)$ , show effects of varying twin-T-cell positive feedback factor,  $m$ , from 0.1 to 0.9.

The gain function of the offered filter according to (Reference 1, Equation 2) has the form:

$$H_{BP}(s) = \frac{V_{BP}(s)}{V_{IN}(s)} = \frac{4RC(1-m)s}{(RCs)^2 + 4RC(1-m)s + 1} \quad (2)$$

where  $m$  is the frequency-independent coefficient of positive feedback supplied to the twin T cell (Figure 1b). The quality factor's value depends on the potentiometer,  $R_{POT}$ , position. At the bottom position of the potentiometer the cursor shows the filter's quality factor  $Q$  at a minimum, and when moving the potentiometer up in position, the quality factor increases.

The positive feedback factor  $m$  is defined as:

$$m = \frac{R_{YZ}}{R_{XZ} + R_{YZ}} = \frac{R_{YZ}}{R_{POT}} \quad (3)$$

The resonance frequency of active filter is:

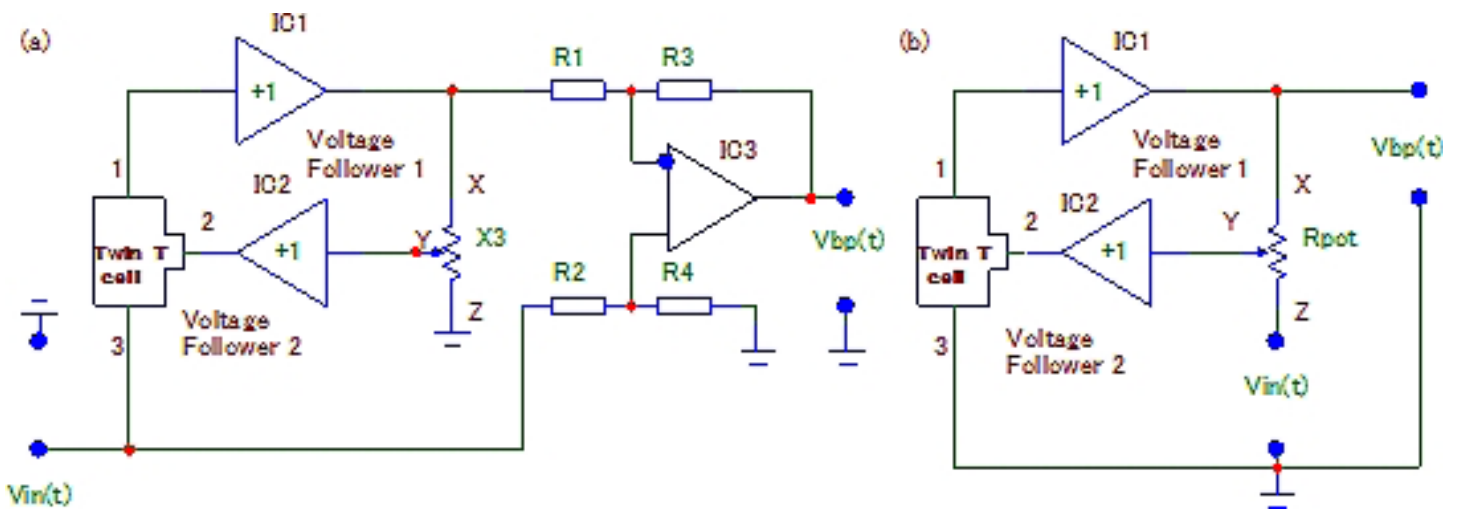
$$\omega_0 = 2\pi f_0 = \frac{1}{RC} \quad (4)$$

The quality factor  $Q$  from Equation 2 is:

$$Q = \frac{1}{4(1-m)} \quad (5)$$

Following H. Martínez et al. [1], the maximum gain,  $A_{MAX}$ , at  $\omega = \omega_0$ , always remains constant and equal to 1 (0 dB) and is independent from  $Q$ . The minimum quality factor is  $1/4$  for  $m=0$ , which corresponds to the potentiometer's rotor connected to





**Figure 3-** Two schemes , which have identical transfer function.  
 (a) - scheme offered by Martinez et al.; (b) - scheme of our design idea.

the input. The maximum gain is theoretically infinite, but, practically, it's difficult to achieve a quality factor beyond 50. In typical applications Q variations are from 1 to 10.

Figure 2 shows Bode plots for the BPF's output,  $VBP(s)/VIN(s)$ , for values of m from 0.1 to 0.9. In the graph, frequency  $f_0$  equals to 1 kHz. Modelling of the filter was done using a circuit simulation program by (ECAD) Micro-CAP 9 of "Spectrum Soft".

Our scheme is obtained by a topological transformation [2] of the original scheme of the notch filter of IC1 and IC2, by transferring the ground wire on the input voltage source  $V_{in}(t)$ .

Thus, the proposed circuit excludes additional differentiating stage IC3 (Figure 3b) and achieved similar results as Martinez et al (Figure 3a).

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*Editor's note: This article was written at the Institute of Experimental Medicine of the North-West Branch of the Russian Academy of Medical Sciences ( IEM NWB RAMS) Saint-Petersburg, Russia*

# DESIGNING FOR IOT—PART IV—THE CLOUD

In this last segment of this series, we will look at back-end services. Some IoT systems may not need back end services like a smartphone controlling a TV, but the majority of the currently envisioned IoT systems rely on the collection, processing and usage of data by the IoT devices and for this, some form of Information Technology different than embedded systems is required.

This article is the conclusion to a four-part series:

- In Part 1, we reviewed the choices facing an embedded developer who needs to build wireless networking into an IoT device (that is, the Thing in the Internet of Things).
- In Part 2, we discussed the different type of IoT devices, and the design choices that you face when designing the hardware and software architectures.
- In Part 3, we looked at the Internet itself, how IoT devices make use of it.

## The Cloud

The Cloud: This is another interesting buzzword. When I was Director of Engineering at Teleglobe Canada, every time we sat in a meeting room to design a network, we drew it as a cloud. A network is a cloud. The Internet is a cloud. And cloud computing is nothing more than an array of networked computers that allow you to offload processing tasks from your embedded system. The same is true for data storage: why store data locally, when you can store it in a secured data centre, with guaranteed power and back-ups?

There is, of course, one fundamental assumption in cloud computing: The network is always available!

So “cloud computing” is a term coined to put a simple name on something that has become very complex. Many companies have launched services that try their best to hide this complexity; these include Apple’s iCloud, Google Cloud Platform, Microsoft SkyDrive, and others. These Cloud computing/storage systems are intended for use with desktop and mobile personal computers. Embedded developers need something similar for IoT devices.

Industry analysts are forecasting the creation of billions of IoT devices by 2020, and these devices will produce huge amounts of data. There are a few approaches for managing and processing all this data.

I see two trends developing among companies that are moving into IoT:

- Some companies are developing and selling their own proprietary solutions because they feel they have the lead, and want to leverage it to its maximum.
- Other companies don’t have the capability to deploy a complete infrastructure, and so prefer to rely on emerging public or commercial solutions.

You can define your own IoT from end-to-end. Many large companies are trying to do just that, and want to capture a good portion of this emergent market. Others are specialising in certain parts, such as GE with its Predix platform for the data

analytics of the industrial internet. Does it mean you absolutely need to buy the provider cloud service stuff? No, you can probably build your own or outsource the expertise you don’t want to build.

Running a backend service must become a core competency for any company attempting to do so; there will be no room for dilettantes. But not all organisations have the DNA to put in place a server farm, guarantee the fail-safe operation of their network, and guarantee data back-ups, system redundancy, and all the crucial things that come with it. Can your system cope with a network failure? If so, for how long?

Early IoT deployment has revolved around sensors and actuators connected to the public Internet via a gateway or hub, and delivering data to an Internet-based server (cloud computing). This is often a vertical integration built around one primary vendor (such as your utility provider and/or telecommunication carrier). All these providers have little or no interest in working together, resulting in an unmanageable melting-pot of services.

The army of devices that compose the Internet of Things will generate more data than any individual Web application. IBM’s chief executive, Virginia Rometty, in The Economist blog “The World in 2014”, provides IBM’s estimates on the quantity of data to be processed in years to come: “By one estimate, there will be 5,200 Gigabytes of data for every human on the planet by 2020.”

In his TED talk: **The Internet of Things is Just Getting Started** [Reference 1], Arlen Nipper calculates that to support the 30 billion connected devices expected to arrive by 2020, we would need to deploy about 340 application servers per day (120,000 servers per year), assuming that we want to deploy all these systems as segregated applications. Mr. Nipper suggests that one way to make IoT possible in the coming years will be to adopt cloud computing.

Around the year 2000, all the telecom carriers claimed that they could each provide the Internet all by themselves. They invested billions of dollars into equipment purchases. Everybody was looking for the “killer application,” the application that would create the “gazillions” of bytes of traffic to fill these networks. At that time, the application that was generating most of the network traffic was e-mail. Today, social media and video sharing are replacing e-mails. When the forecasted traffic did not materialise on this huge IP network, it triggered the dot-com bubble burst.

With IoT, we are finally seeing a new “killer application.” When billions of devices exchange information over the Internet, they will require significant network bandwidth, and especially enormous data storage and processing capabilities. A new term has been coined lately to represent this new trend: Big Data.

*In the continuation of this article, the author looks at backend services, and the contention that “every company will become a software company” - click right.*



# ENSURING DIGITAL DISPLAYS FLOURISH IN ALL CONDITIONS

Today, wherever we go, information is at our fingertips – whether it comes from indoor equipment, outdoor kiosks, or the smartphone in our pocket. This penetration depends heavily on the equipment and devices’ display and touch interfaces; can these UIs effectively deliver an engaging and reliable experience, withstanding challenges from any environment they find themselves in?

Below, we look at these challenges and the technologies to counter them. We then draw on andersDX’s extensive experience with supplying UIs into widely varied applications to show these technologies working in practice.

## Display enhancement requirements and solutions

Display enhancements are typically needed to accommodate and compensate for glare and sunlight, fingerprints and scratches, shock, vibration and malicious attack, and temperature extremes. Additionally, as displays become increasingly interactive, any enhancements must be complemented by suitable touch screen solutions. Other issues including humidity, water and dust ingress can be solved with suitable, and well-established, enclosure designs.

Circular Polarisers provide optimal sunlight readability, cutting total light reflections to 1% of incident light. Sunlight readability can also be improved by applying anti-reflection optical films or coatings combined with optically-clear glue between the display’s surface and the transparent protective layer. This can yield further reductions in total reflections to as low as 0.2%, resulting in a perceived increase in display contrast of some 300%. Anti-glare films reduce glare that can originate from over-head lighting, for example, by diffusing concentrated beams of light to levels far less distracting to the user, while increasing light output of a display’s backlight unit to deliver a front of display luminance of around 1000nits or above, which will greatly contribute to improved sunlight readability.

Challenge	Solution	Comment
Readability in bright sunlight and glare	Optical bonding	Contrast up to 10:1, 300% improvement in impact resistance
	Polariser	Cuts total light reflection to 1% of incident light
	Anti-reflection optical film	Increases contrast ratio up to 300%
	Anti-glare film	Improves contrast ratio, reduced surface reflections
	LED backlight	3 x increased light output
Impact resistance	Optical bonding	See above
	Safety glass	Excellent for vandal resistance
	Anti-smudge screens	Reduce fingerprints and scratches
Privacy	Privacy filter	Limits viewing angle to 48° or 60°
Overheating in strong sunlight	Heat mirror	Rejects up to 90% of incident solar energy
Extreme cold environment	Transparent heater	Extends operating temperature down to -50°C
Touch technologies	Resistive	Early technology, still highly favoured in industrial applications
	Projected capacitive	Provides good user experience, popularity accelerated by use in smart devices
	Shadowsense	More recent technology, highly accurate and cost-effective

Table 1 summarises the UI challenges and enhancement solutions available.



Optical bonding, the term that describes the clear-gluing process mentioned above, is highly effective in outdoor and public environments. As well as improving contrast ratios to 10:1, it provides up to three-times better impact resistance. Safety glass is also available to provide an excellent level of vandal resistance, while anti-smudge screens reduce everyday fingerprint and scratching issues. For applications such as ATMs where privacy is required, privacy filters are available that limit full-field viewing angles to 48° or 60°.

Where strong sunlight creates heating as well as readability problems, a heat mirror can keep displays cool. By reflecting infrared radiation, these can reject 90% of incident solar energy. Conversely, a transparent heater can be used to warm displays in extremely cold environments, extending operating temperatures down to -50°C.

Different touch technologies are available for interactive UIs. Resistive touchscreens are preferred where low cost and low emissions take precedence over ease of use. 4-wire types are standard, with 5, 6 and 10-wire solutions available as alternatives for enhanced robustness. They can be integrated with a coverlens for aesthetics and protection. PCAP Projected Capacitive touchscreens offer greater accuracy and an “iPad-like” user experience together with thinness, low weight, great durability, and multitouch capability. A recently-introduced technology – ShadowSense – offers a scalable and robust solution with drift-free performance, outstanding optical clarity and a fast, accurate response time. This optical touch technology, implementing multitouch detection from the periphery of the display, is reliable, durable and attractively-priced.

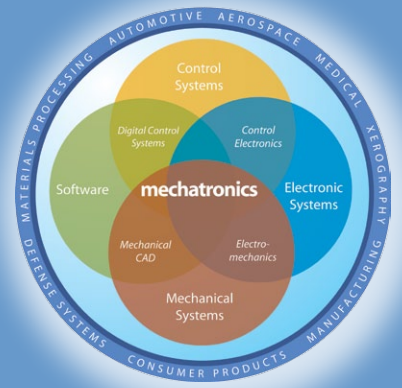
## Real-world display enhancement examples

Because real-world applications are so diverse, finding the right UI products and engineering them into their target system takes innovation and flexibility. For example, an indoor environment is not necessarily benign; a recent UI project concerned a professional catering oven subject to the heat, humidity and rough handling of a busy kitchen. Read more about the engineered solution, and others - click right.



# MECHATRONICS IN DESIGN

FRESH IDEAS ON INTEGRATING MECHANICAL SYSTEMS, ELECTRONICS, CONTROL SYSTEMS, AND SOFTWARE IN DESIGN



## Control, control, you must learn control!

Kevin Craig

Over 20 years ago, while teaching at Rensselaer Polytechnic Institute, my colleagues and I, working in the emerging field of Mechatronics, came to understand the importance of integrating control in the design process from the very start of the design process.

Adopting a model-based design approach made this integration easy indeed, accessible to all engineers with some education in control fundamentals and their application to real engineering systems. The increase in the power of microelectronics and the decrease in their cost has now made possible, in everyday systems, the application of control approaches found only in research labs a few years ago. Yes, now control is an indispensable technology in modern multidisciplinary engineering practice.

Alas, you would not come to that conclusion reviewing the engineering curricula at universities or speaking with most practicing engineers today who are products of those programs. Modelling and control make physics and mathematics relevant and necessary for the engineering student and this message needs to be delivered on day one. Why is this not so? If you have an answer, please let me know.

Classical Control Theory (root-locus and frequency response analysis and design, i.e., transform methods) is applicable to linear, time-invariant, single-input, single-output (SISO) systems. This is a complex frequency-domain approach. The transfer function relates the input to output and does not show internal system behaviour.

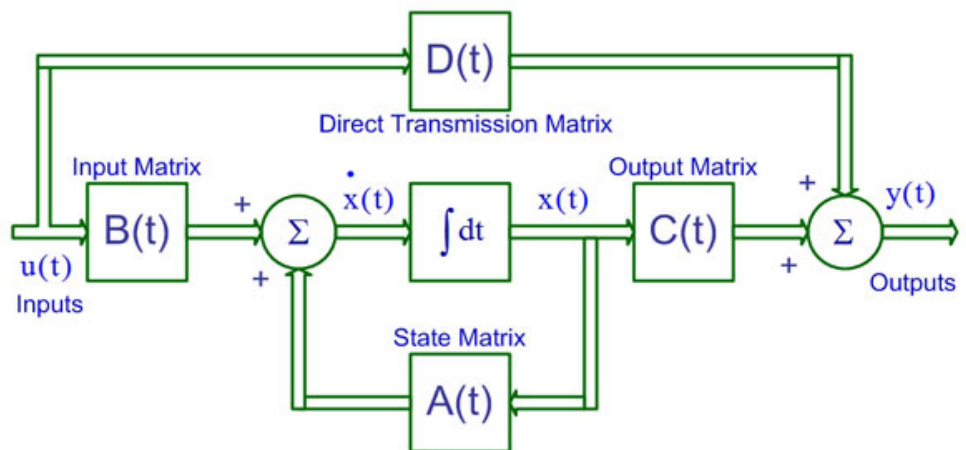
Modern Control Theory (state-space analysis and design) is applicable to linear or nonlinear, time-varying or time-invariant, multiple-input, multiple-output systems. This is a time-domain approach. This state-space system description provides a complete internal description of the system, including the flow of internal energy.

The aim of both techniques is to find a controller that satisfies the design specifications. Knowledge of both approaches, modern and classical, is essential to produce the best designs.

Even when control is taught, the subject of state variables

and state-space control design is rarely covered. While classical control, specifically proportional-integral (PI) control, accounts for about 90% of the industry applications, that is rapidly changing. State-space control is now essential for many applications to just function.

The state-variable equations (see diagram) are a coupled set of first-order ordinary differential equations where the derivative of each state variable is expressed as an algebraic function of state variables, inputs, and possibly time. The state variables



are independent variables capable of defining the state from which one can completely describe the system behaviour. These variables completely describe the effect of the past history of the system on its response in the future.

Choice of state variables is not unique and they are often, but not necessarily, physical variables of the system. They are usually related to the energy stored in each of the system's energy-storing elements, since any energy initially stored in these elements can affect the response of the system at a later time. The internal energy can always be computed from the state variables. The number of elements in the state vector is unique, and is known as the order of the system.

Advantages of state-space design are especially apparent when the system to be controlled has more than one control input or more than one sensed output, the multiple-input, multiple-output (MIMO) system case.


Yoda was right and his words need to be heeded today more than ever before.

# designideas

READERS SOLVE DESIGN PROBLEMS

## Versatile noise generator tests signal recovery gear

Vladimir Rentyuk

 I sometimes need a noise generator for testing equipment, and useful signals must often be mixed with the noise, such as when testing equipment designed to extract a clean signal from a contaminated one. This Design Idea implements such a piece of test equipment.

The source of white noise is avalanche diode D2 (Russian 2Г401B): the spectral density of the noise is not less than  $30 \mu\text{V}/\sqrt{\text{Hz}}$  @  $25 \pm 10^\circ\text{C}$ , and irregularity of spectral density less than 4dB from 20 Hz to 1 MHz.

The SSM2166S microphone preamp and compressor (IC2) (with "A" mark on package; without "A" needs another adjustment – see the datasheet) provides normalization of RMS noise level. The compressor stabilises the output noise level at 775 mV RMS (0 dB), even as the input of IC2 varies from 3-30 mV – much more variation than that expected from D2.

A filter can be placed between D2 and C2 if desired. In my generator, a 4th-order Butterworth LPF at 5 kHz is used. Without the filter, the frequency range of the noise will be approximately 20 Hz-20 kHz as set by IC2 & IC3.

Output level can be adjusted by R22 & R7. Values of the other parts around IC2 were established experimentally, by criteria of

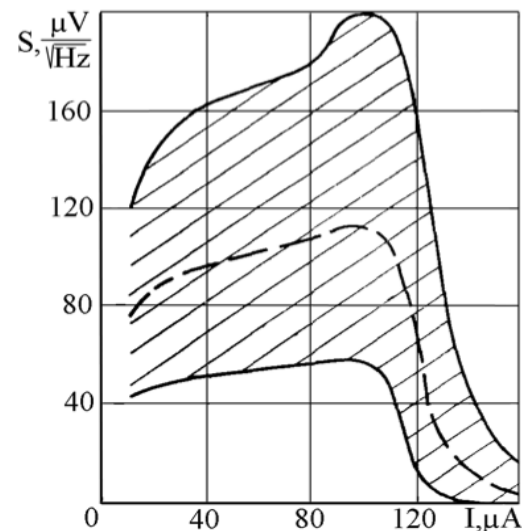


Figure 2. The spectral density of the 2G401V vs. operating current

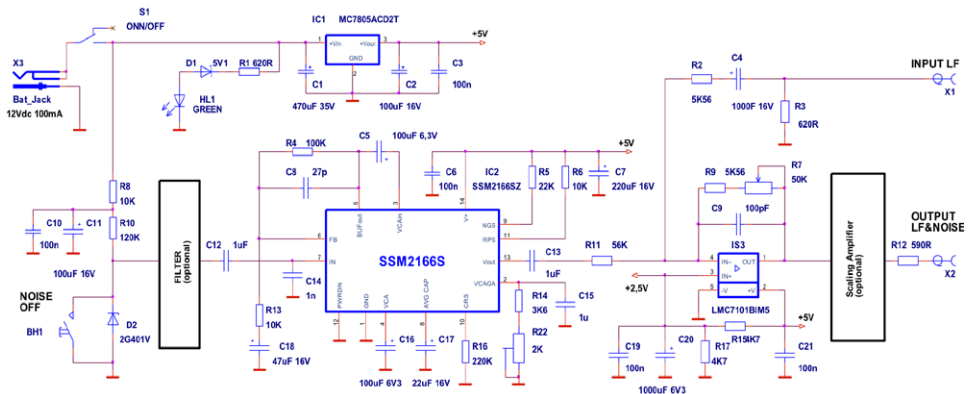


Figure 1. Noise generator schematic

stability of characteristics of the generator (additional gain in its buffer amplifier: 20 dB, compression ratio: 15:1, total gain: 34 dB, rotation point: 150 mV, noise gate: 10 mV). The standard output resistance of  $600\Omega$  is established by R12 and the output stage resistance of the generator.

The test generator allows mixing of noise signals with another signals, for example, a low-frequency sine. The external signal is connected to the X1 "INPUT LF" socket. The switch BH1 turns off the noise signal, letting only the clean input through.

The signal level can be reduced in decade steps using an additional scaling amplifier. Switches S2-S5 select the gain.

The generator uses power from an external PSU of 12 VDC at 100 mA.

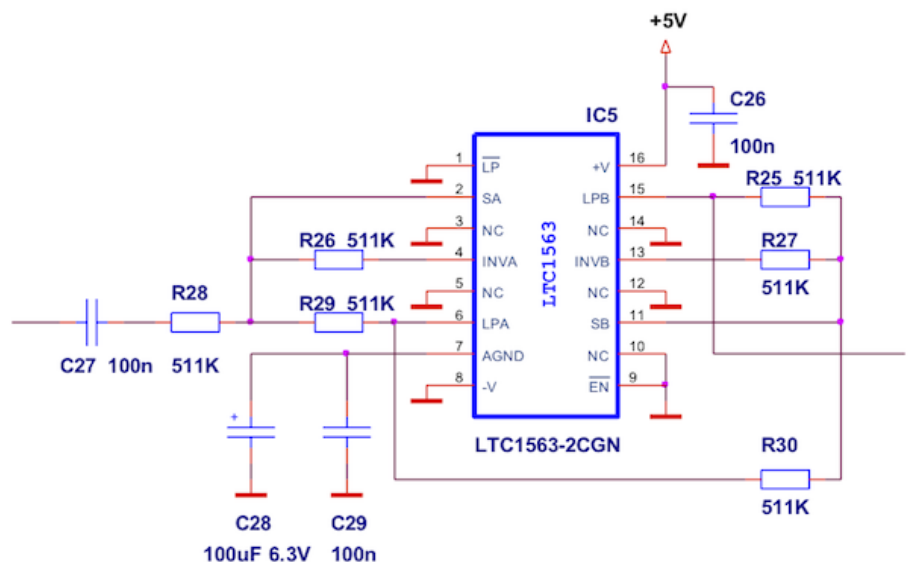
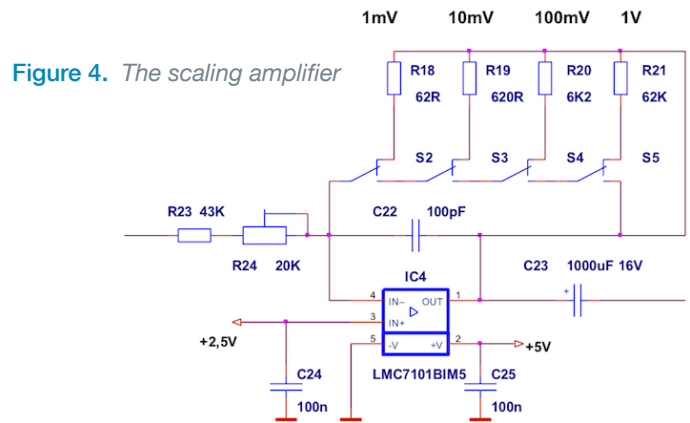


Figure 3. The optional 4th-order 5kHz Butterworth LPF

Vladimir Rentyuk is a development engineer at Modul-98, a developer of embedded electronic systems, robotic equipment, image recognition systems, and other products for European and world markets. He holds a master's degree in radio engineering from Zaporizhzhya Machine Construction Institute (now Zaporizhzhya National Technical University) in Ukraine.



## Failsafe multichip LED module driver

Subodh Johri

The operational life of an LED depends upon how effectively the current flowing through it is kept within the specified limits under all possible working conditions. For multi-chip LED modules, the tightly binned LEDs are arranged in strings having multiple LEDs connected in series, parallel, or series-parallel configurations, sharing a common constant current or voltage source, and each LED string is typically driven at a regulated current that is substantially equal among all of the LED strings. Although a small imbalance in string currents does not cause noticeable differences in brightness, parameters like the compound forward voltage (sum of  $V_F$  of all LEDs connected in series), and its critical dependence on temperature and magnitude of forward current ( $I_F$ ) flowing through it, besides other process dependent variations, make the current balancing a tough task over the long period. Also, as a result of the failure of any LED(s), string(s), or the possibility of LEDs being leaky or less efficient due to hot spot formation, may further impose more burden on these and lead to shortening of life and ultimately catastrophic failure of the SSL and its associated driving source.

The motive behind developing this driver was to provide an efficient and fault tolerant workhorse especially for integrated LED modules comprising medium and high-power LEDs configured in series or series-parallel combination. Unlike Solid State Lights made out of

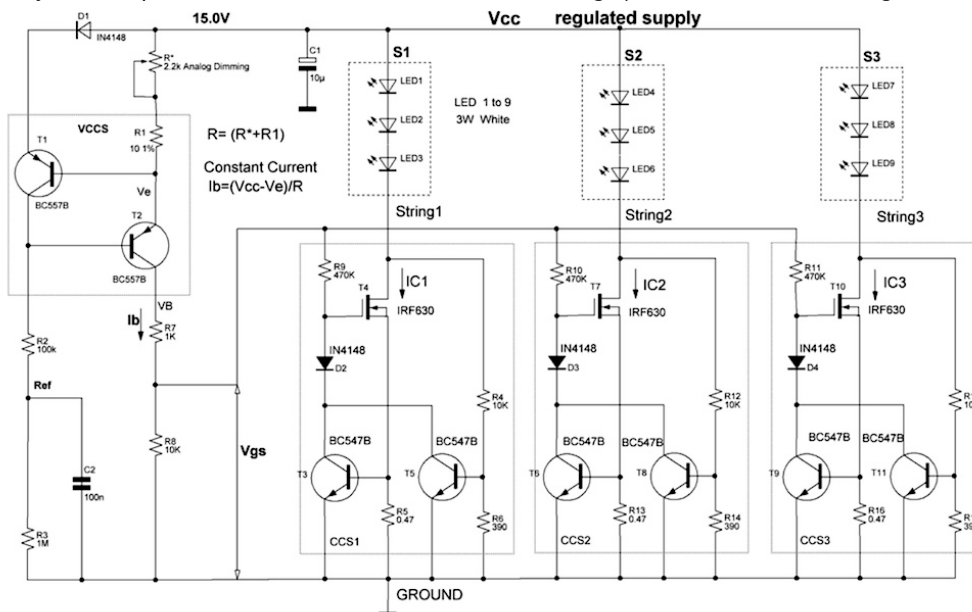
discrete power LEDs, the integrated LED chip has no room for replacement/repair of any faulty LED if it becomes open, shorted, or leaky due to electrical or thermal stress encountered during its operation. The circuit handles such mishaps and isolates the faulty string(s) without imposing any penalty on power budget or affecting other strings working normally.

The proposed Design Idea uses a technique which allows the parallel-driven LED strings to work within a specified regulated current range by precisely injecting a reference current ( $I_B$ ) into multiple current sensitive switches to which LED string are tied, and accordingly adjusts its magnitude under normal and anticipated electrical faults, which might occur during its life time, and thus provides fault tolerant protection from imbalance of current in LED strings during short circuit, leaky, or open circuit conditions. Unlike other circuits, the simplicity, cost effectiveness, and efficiency of the circuit facilitates many additional advantages besides its ingenuity.

The circuit consists of three LED strings, S1, S2, & S3, each having three series-connected 3W white LEDs connected to MOSFET/BJT based constant current sinks (CCS). The current ( $I_{C1}...I_{C3}$ ) flowing into each string is determined by the constant current  $I_B$ , generating  $V_{GS}$ , which is applied simultaneously to the gates of all the MOSFETs. The constant current  $I_B$  sets the gate to source voltage  $V_{GS}$  to T4, T7, & T10. T3 (we'll just consider String 1) limits the current through the sinks as soon as the potential drop across R5 approaches 600 mV, thus reducing gate drive.

Another feature has been incorporated into each current sink by wiring T5 in parallel with T3. Normally T5 remains off until drain voltage rises close to  $V_{CC}$ , producing sufficient voltage across R6 to drive T5 into saturation to de-energise the MOSFET by grounding the gate.

The position of  $R^*$  controls the magnitude of the constant current ( $I_B$ ) in a voltage controlled current source ( $V_{CCS}$ ) configured around T1, T2 & ( $R1+R^*$ ) and accordingly generates the appropriate  $V_{GS}$  to drive MOSFETS, but additionally it provides an analog current dimming feature. The Ref node in the schematic has been provided as an emergency shut off feature to disable all the strings by



applying a voltage close to  $V_{CC}$ , pushing constant current  $I_B$  to zero.  $I_B$  is equal to:

$$I_B = (V_{CC} - V_e) / (R1 + R^*)$$

Performance: The normal string current has been set around 1A for the given component values. It can be seen that the worst case current normally remains around 1A, except cases where string current falls to a few mA or becomes negligible during extreme leaky, short, or open circuit conditions.  $I_B$  can be varied from 0.4 mA to 1.4 mA for the given component values. If needed, the string current can be increased by reducing the sense resistor R5 appropriately. The LEDs and power MOSFETs must be mounted on suitable heat sinks/metal core PCBs to


avoid thermal runaway.

Protection against short circuit: If any LED(s) in a particular string gets short circuited, the SSL would continue to work normally, however, if the entire string gets short circuited, the potential at the drain of the MOSFET will rise to  $V_{CC}$  and in such condition the respective MOSFET will be disabled, forcing drain current to zero.

Protection against leaky LEDs: If any LED(s) in a particular string gets leaky, it would continue to work normally, however, if entire string gets leaky, the drain of the MOSFET will rise to  $V_{CC}$  and in such condition the MOSFET will be disabled, forcing drain current to zero.

## Avoid problems with multiple DC-DC converters

Michael Dunn

 Most electronics today requires multiple supply voltages – four or more rails is not uncommon. But if you're using multiple, unsynchronised DC-DC converters, you've not only

eliminated caps. The improved performance is a free bonus.

Fortunately, many IC and modular converters these days have a SYNC input pin. The LM2747 is a good example of a suitable

controller IC. The synchroniser is a CMOS decoded counter, such as the 4017/4022, or 74HC4017. This is driven with a clock signal equal to the converters' operating frequency times the number of converters. Connect the first unused counter output to its RES/MR (master reset) pin to set the correct count length.

This design can easily be implemented in programmable logic too, potentially making it totally free. Of course, the switchers won't be synchronised as the power is ramping up. The synchronisation logic will need to reach its operating voltage, and the converters themselves may have a small sync-up delay. If an FPGA is

used for control, it may also require time to initialise.

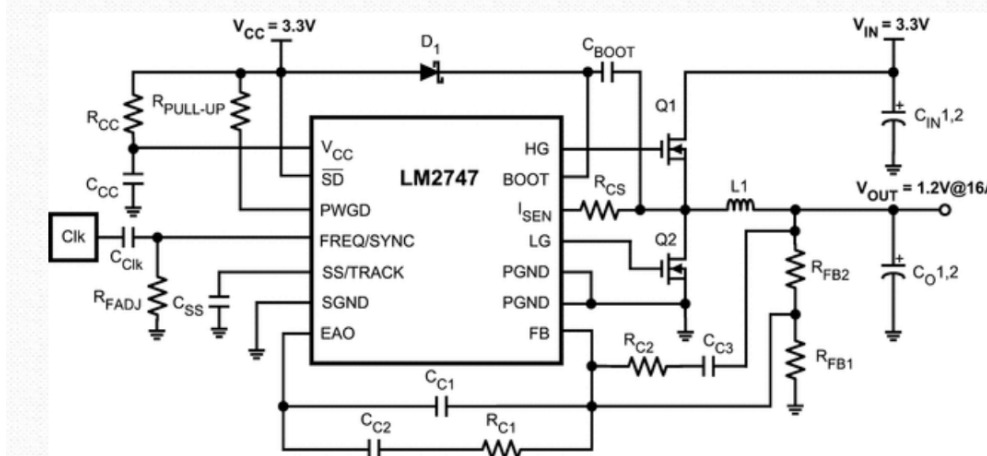


Figure 1. Example DC-DC converter with SYNC input

got a sub-optimal design, you're asking for trouble. This Design Idea solves both problems.

Why trouble? I have first-hand experience of multiple power frequencies used in a system which also included sensitive analogue electronics. Under certain conditions, difference frequencies (e.g., 10 kHz, if one switcher was running at 250 kHz, and another at 260 kHz) would show up in high-impedance analogue sections. Not good.

Why sub-optimal? The input filter capacitors of a DC-DC converter are almost as critical as the output caps. These capacitors, be they large ceramics, or high-performance electrolytics, are not cheap. In a multiple-converter system, each converter will need a full complement of input capacitors. But if we synchronise and stagger the channels, input capacitors can be "shared" to some extent. The cost and size of the circuit presented here could easily be less than the cost and size of the

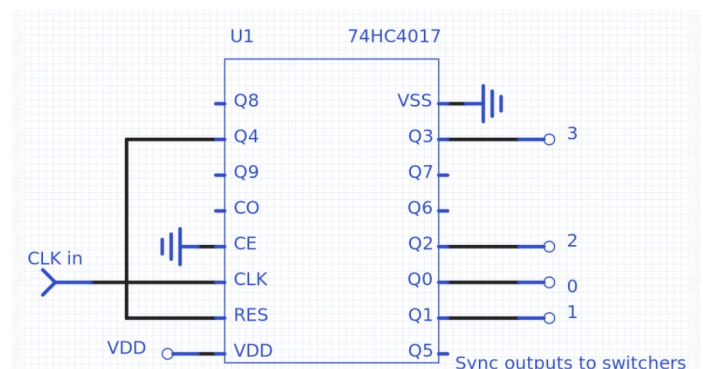


Figure 2. Synchronisation circuit wired for four converters

# productroundup

## Low-profile power MOSFET package

Infineon has introduced a leadless surface mounted package for its CoolMOS MOSFETs; ThinPAK 5x6 is intended to expand the use of these FETs in adapters, consumer electronics and lighting applications. With its height of 1 mm and with its small footprint of 5 x 6 mm the ThinPAK 5x6 provides 80% volume reduction in comparison to traditional SMD packages such as DPAK. The very low parasitics of ThinPAK – such as low source inductance compared to the traditional DPAK – reduce the gate oscillation under all load conditions and minimise voltage overshoots during switching by 40% in comparison to traditional SMD thus improving device and system stability and ease of use. ThinPAK 5x6 offers engineers more flexibility in their PCB designs and better switching performance; it follows the earlier release of the ThinPAK 8x8 for higher power applications such as server and telecom SMPS.



Complete article, here

## Solar micro inverter development kit provides complete hardware and software

To simplify design for solar power applications, Texas Instruments' C2000 Solar Micro Inverter Development Kit implements a complete grid-tied solar micro inverter based around TI's C2000 Piccolo TMS320F28035 microcontroller. Solar micro inverters are an emerging segment of the solar power industry. Rather than linking all solar panels in an installation together to a central inverter, solar micro inverter systems place smaller, or "micro," inverters at the output of each individual solar panel. The kit implements control of an active clamp flyback DC/DC converter with secondary voltage multiplier, MPPT and a grid-tied DC/AC inverter, comprising the power conversion stages of the solar micro inverter: it supports panel voltages of 28 to 45V at input as well as universal power output at up to 280W for 220VAC and up to 140W for 110VAC, making it suitable for worldwide solar markets.



Complete article, here

## Runtime analysis for ARM code

Fully integrated with IAR Embedded Workbench for ARM, C-RUN is an add-on product that provides developers with access to code analysis. The C-RUN runtime analysis product is available as an add-on to the IAR Embedded Workbench for ARM development toolchain. Integrated with the toolchain,

C-RUN offers each developer access to runtime analysis. C-RUN is a new product from IAR Systems that performs runtime analysis by monitoring application execution directly within IAR Embedded Workbench. Tight integration with the toolchain sup-

ports the full cycle of implementation, testing and debugging. C-RUN for ARM has several features such as bounds checking to ensure accesses to arrays and other objects are within boundaries, different overflow and arithmetic checks, as well as a comprehensive heap checker.



Complete article, here

## Forth for ARM Cortex-M and TI MSP430: free compilers

Microprocessor Engineering (MPE) is a promoter of the Forth language, and contends that Forth offers faster coding and testing. Acknowledging that most work with Forth in recent years has been in niche applications, MPE sees it as gaining traction and in its support, is now offering free versions of the Compiler for established DevKits to enable engineers to try it out. Forth is available for ARM Cortex-M and TI MSP430 cores. The new, free, Lite compilers are targeted at standard Development Kits, providing developers of high integrity embedded systems with a fast route to prototyping. The Forth programming language is suitable for applications where interactive programming, fast time to prototypes and incremental code generation are needed. High integrity system requirements are increasing in Medical, Rail, Automotive and Robot applications, where the most resilient and robust development processes are called for. Forth is well suited for such applications, MPE asserts. The Lite compilers provide a complete integrated set of tools (unlike other languages). They include conventional cross-compilation as well as a complete Forth system resident on the target microcontroller. The Lite compiler's IDE and terminal emulator run on a PC, making remote servicing easier. Code generated is directly compiled into the microcontroller's Flash memory. A USB connection, or even an RS232, is sufficient for in-the-field changes; software can be adapted and code changed, without using any additional tools, making the compiler ideal for testing set-ups and for field service.

Complete article, here



## Digital-lighting MCU is state-machine based

The STLUX development environment, consisting of demonstration boards, a graphical configurator, software libraries, and compiler, provides everything needed to start designing high-performance LED lighting with STLUX385A, the first in a new family of lighting controllers featuring a new

**STLUX™**  
Development Environment

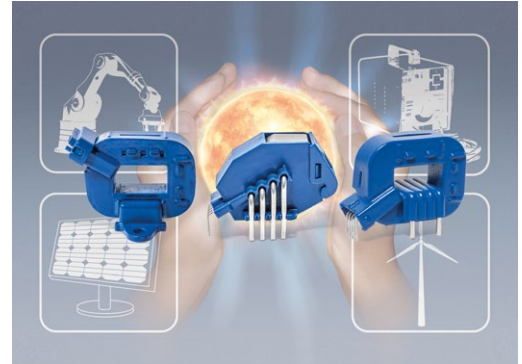


digital control technique from STMicroelectronics. The STLUX development environment is demonstrated with a plug-and-play demonstration board featuring all STLUX385A functionalities and a context for programming PWM waveforms using the six on-chip SMED (State Machines Event Driven) digital controllers. The SMED is an advanced hardware-configurable state machine where state advancement is automatically triggered by internal or external events thereby ensuring faster response than a conventional interrupt-driven micro-processor. STLUX385A supports smart-grid connectivity and DALI communication for remote control.

Complete article, here

## Open-loop Hall-effect transducers measure to 250A

LEM has extended the measurement range of its HO series current transducers up to 250A; at the same time it has further improved the specifications which continue to edge close to what is achievable with the – more complex and costly – closed-loop techniques. These moulded components are configured either with primary conductors installed, for PCB mounting; or with apertures that accept a primary conductor (cable). Using LEM's in-house-designed



ASIC, they measure up to 250A DC, AC or pulsed, with over-current detection and fault reporting, over an operating temperature range from -40 to +105°C. By orienting a single snap-on moulding in different positions, the same unit can be panel-mounted in different orientations or can be locked to a busbar that is the primary conductor. HO series current transducers measure DC, AC, and pulsed signals using the latest generation of LEM's Open-loop Hall-effect ASIC.

Complete article, here

## 40-V MOSFETs cut on-resistance

Toshiba Electronics' latest family of low-voltage Trench-MOSFETs is based on the company's U-MOS IX-H process and further improves the on-resistance-to-output-charge-product figure of merit for this class of devices. Initially available in 40V versions, the family will be extended in the coming months with

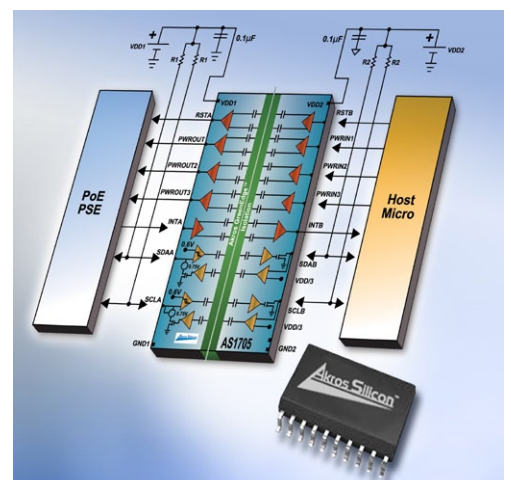


devices offering ratings of 30V to 60V. The first device in the series has a typical RDS(ON) of 0.7 mΩ (max 0.85 mΩ) and a typical output capacitance (Coss) of 1930 pF. Rated for 40V, the TPHP8504PL is supplied in an SOP-Advance package measuring 5 x 6 mm. Target applications for the ninth generation U-MOS family include DC-DC converters, synchronous rectification and other power management circuitry. U-MOS IX-H MOSFETs are suitable for high-side and low-side switching in DC-DC converters and secondary side synchronous rectification in AC-DC conversion circuitry.

Complete article, here

## 7 channel, 3.4-MHz isolator for I<sub>2</sub>C

Akros is a fabless semiconductor supplier that specialises in Power-over-Ethernet. It has taken the signal isolation technology it developed for the control channels of PoE and packaged it as a dedicated isolator, that expands the company's GreenEdge digital isolation technology into the PSE segment of the PoE market, enabling real-time energy management in network systems. The AS1705 is the only such product to feature 3.4 MHz communication speed, Akros says. The AS1705 comprises a dual channel bidirectional I<sub>2</sub>C digital isolator as well as five unidirectional channels of isolation. Each of the isolation channels is rated to provide 2.5 kV of galvanic isolation. On the bidirectional I<sub>2</sub>C channels, the AS1705's 3.4 MHz data rate provides the needed bandwidth for a system's processor to dynamically monitor and control the power requirements for multiple PSE controllers within a system.

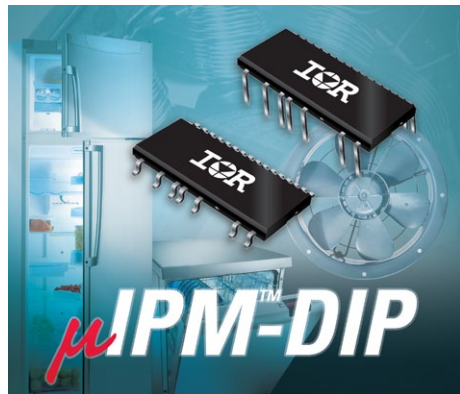


Complete article, here

## Motor-drive integrated module packaged in DIP

International Rectifier has introduced the  $\mu$ IPM-DIP family of highly integrated, compact Integrated Power Modules (IPM) for low power motor drive applications. IR previously launched the  $\mu$ IPM Power Modules in a highly-integrated and miniature surface mount package format. The company is now offering the same electrical feature set in a format that it says will be easier to

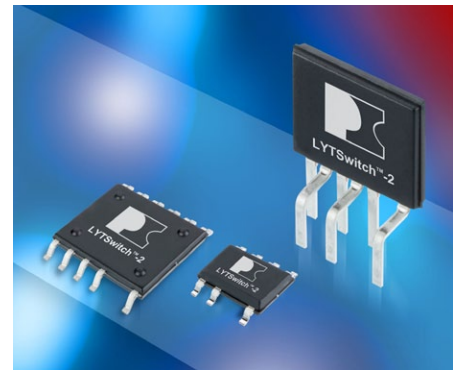
handle for some of its customers. A company spokesman noted that not all designs need the very small outline of the surface-mount version. Now in a 12 x 29 mm SOP/DIP package, the  $\mu$ IPM-DIP product family offers a cost effective power solution by using industry standard footprints and processes compatible with various PCB substrates. The family of 32 new devices uses rugged and efficient high-voltage FredFET MOSFETs optimised for variable frequency drives with voltage ratings of 250V or 500V to drive motors up to 150W.



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## Isolated LED-driver ICs boost power & accuracy

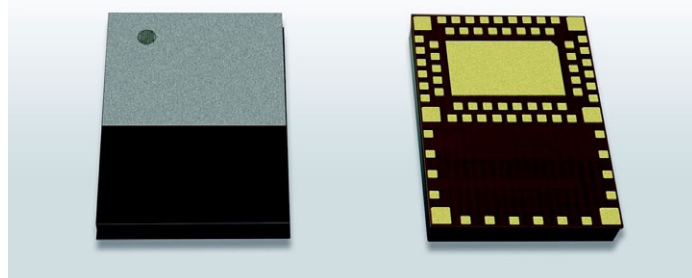
Power Integrations' LYTSwitch-2 family of isolated LED drivers delivers up to 12W of accurately controlled output power, reduces component count, and enables simpler, smaller, more reliable LED lighting designs. LYTSwitch-2 LED-driver ICs use primary-side control, resulting in cost-effective, single-sided PCBs with low component counts. Driver isolation allows the LEDs to be attached directly to a metal heat sink, avoiding an electrically isolating enclosure that is often required for non-isolated drivers. Accurate constant-current (CC) output tolerance across temperature (better than  $\pm 5\%$  at both low-line and high-line voltages) reduces the need to over-design systems in order to meet requirements such as the U.S. ENERGY STAR minimum-lumens-delivered specification. Designs using LYTSwitch-2 ICs are also highly efficient – up to 90% in typical applications. Transition from CC to CV operation is automatic, depending on the load presented to the driver.



Complete article, here

## Bluetooth Smart SiP “drop-in” module

Based on the Nordic Semiconductor nRF51822 System-on-Chip, the ISP130301 from French system-in-package specialist, Insight SiP, is a drop-in solution that requires only a 2.1 to 3.6V on-board power source and sensor (if applicable), and can run up to several years from a coin cell battery. The Insight SiP ISP130301 measures 8 x 11 x 1.2 mm and is positioned as a complete 'drop-in' Bluetooth Smart module solution for developers of “accessory” products. Nordic Semiconductor and



Insight SiP say the module requires no specialist RF engineering experience. In a QFN, LGA package the module includes, in addition to the nRF51822 and its 32-bit ARM Cortex M0 microprocessor, 256 kB of Flash memory, and full suite of analogue and digital peripherals (including 2-wire, ADC, AES, GPIO, PWM, Real Time Clock, RNG, SPI, Temperature Sensor, and UART), a DC-DC converter, integrated RF antenna, 16 MHz and 32 kHz high stability quartz oscillators, plus an RF matching circuit and passive components.

Complete article, here

## Lantq uprates SHDSL for industrial DSL

Lantq, supplier of chips and software for broadband access and home networking, has announced an SHDSL initiative, designed to bring the unique data-rate and reach performance of G.SHDSL and Ethernet First Mile (EFM) to new applications. The company comments that 15 years after its first market introduction, SHDSL has gained a second life in industrial applications. A new firmware version (V 1.9) for the Lantq SOCRATES SHDSL chipset provides substantially enhanced interoperability. Lantq is launching an SHDSL CPE test service program, providing customers with sophisticated test capabilities from the Lantq Labs. To meet the long-term product availability requirements for industrial markets, Lantq is committed to mainstream manufacturing technologies to achieve the best possible product lifetime. The four-channel SOCRATES SHDSL products also have been converted from gold to copper bond wiring, with samples available now.



Complete article, here

## Wireless USB IC targets 3-year battery life

Cypress Semiconductor says that its ultra-low-power 2.4-GHz WirelessUSB NX transceiver enables three-year battery life for wireless human interface devices, while supporting data rates of up to 2 Mbps, and allowing integration with Cypress's touch sensing technology. The fourth-generation 2.4-GHz WirelessUSB radio-on-a-chip is for wireless mice, keyboards, trackpads, remote controls and other Human Interface Devices (HIDs).

WirelessUSB NX operates at 900 nA in sleep mode where HIDs spend most of their time, and it offers active current of 12 mA in transmit mode and 15 mA in receive mode. The NX radio offers superior performance in the presence of common 2.4-GHz interference from sources such as WiFi, Bluetooth, cordless phones and microwaves. WirelessUSB NX is complemented by Cypress's highly integrated enCoRe VI microcontroller, PSoC 4 system-on-chip devices and complete trackpad modules for touch interfaces.



[Complete article, here](#)

## High-accuracy temperature sensor

Sensirion's STSC1 temperature sensor combines high measurement accuracy with an attractive price-performance ratio, low power consumption and minimal size. The STSC1 focuses on applications that require very precise temperature measurement. It is suitable for consumer electronics, Internet of Things and smart home applications, as well as for data loggers and thermostats.

With compact dimensions of 2 x 2 x 0.8 mm, low power consumption and supply voltage of 1.8V, it provides a fully calibrated and linearised digital signal to a microcontroller. The device measures temperatures from -40 to 125°C with a typical accuracy of  $\pm 0.3^\circ\text{C}$ . The fully calibrated sensor features an I<sub>2</sub>C interface and is reflow-solderable. It is suitable for standardised industrial series production of electronic devices and can be successfully integrated into complex applications.



[Complete article, here](#)

## Optical sensor optimises display performance

ams' integrated colour sensor drives intelligent display management in smartphones and tablets; the TMD3782 digital sensor is intended for use in mobile devices and combines ambient light, colour and proximity sensing. Positioned as the first integrated ambient light, colour (RGB) and proximity sensor that is optimised for operation behind dark glass to drive intelligent display

adaptation in mobile devices, the TMD3782 optical module is suited for smartphones and tablets. The sensor integrated in the TMD3782 provides ambient light intensity (lux) and colour measurement enabling mobile devices to automatically adjust their display's colour and brightness for the best viewing experience and power savings. The device is able to sense light in a similar manner to the human eye, enabling more sophisticated control of the display brightness and colour. The TMD3782 packs the ambient light, colour and proximity sensor, IR LED and optical lenses in a 3.9 x 2.4 x 1.4mm module.



[Complete article, here](#)

## Sapphire trimmer cap, non-magnetic for MRI use

Voltronics has added to its range of non-magnetic trimmer (variable) capacitors; the company claims to have the widest range of such products for Magnetic Resonance Imaging available. V9000 series is the company's smallest, high voltage trimmer capacitor. The V9000 Sapphire trimmer capacitor is sub-miniature at 16.3 mm (at minimum capacitance) in length, but offers the highest

working voltage rating (2 kV) for its size - whilst delivering a capacitance range of 1 to 12pF. Sapphire is ideal for precision trimmer capacitors as its dielectric constant is extremely stable, measuring below 0.0003 up to 10 GHz, and is chemically inert; totally moisture resistant and mechanically strong. These trimmers have a high Q (3000 min at 100 MHz); DC working voltage of 2000V and DC withstand of 3000V. The V9000 Series is designed for the MRI industry where its size, power, capacitance range and affordability make it the preferred choice for the next generation of coils.



[Complete article, here](#)

# Don't send a man to do a meter's job

I was once part of a group of young engineers working on a Hi-Fi stereo-monoblock music centre, which consisted of a tape recorder, a player, an all-wave broadcasting receiver, a power amplifier, and a preamplifier with sensor control. Our work was interesting, but some of the requirements of national standards in the USSR in the early 1980s were stumbling blocks. One of these standards provided requirements for consumer electronics quality.

I agree that the quality of any equipment should come up to the mark. If a specification says that a signal-to-noise figure-of-merit must be no less than 70dB, it must be, but one of our standards included a requirement about audio-hearing control that was to be tested by ear.

Personnel from the quality control department used headphones to test each music centre. You can agree with me that it is difficult for people without a delicate ear for music to feel all nuances of music, but this testing was presented in our situation because the factory never manufactured musical equipment before.

I can say that almost everyone in the quality control department had tin ears. We had high-pitched arguments with them about this problem. They would argue that they may not feel all nuances of music, but they could hear! They said that hearing noise does not need a delicate ear for music, and unfortunately all of our big bosses agreed. This caused a real headache, because this testing was very subjective.

One day, our team of development engineers headed to the assembly shop because the engineer of the quality control department again heard noise while checking a device. I brought measuring equipment and showed that the level of noise was in the specific norm with a good margin, but the engineer said, "I hear noise and this device will be condemned." I again showed the specification and measurement of the signal-to-noise. All was in the norm, but he said that the standard requirement was to check devices by hearing and he heard strong noise. Our manager and one from the quality control department had to be called in.

Many people stood near this music centre and checked the noise of the device by ear. One of our engineers asked, "Which of the channels has more noise?" The quality control engineer answered with confidence, "The most

noise is in the right channel." We asked him listen once again, very thoroughly. He was still sure that the noise in the right channel was more and it had an inadmissible level. The head of quality control took stereo-headphones too. He heard noise and confirmed the fully inadmissible noise in the right channel.

Before the test, our engineer disconnected the control headphones and placed the connector in his pocket. We showed them that the headphones were connected to the pants pocket of our engineer, not the product, all this time. It was a shock!

I understand it wasn't the best idea for young engineers to fool the managers, but all's fair in love and war, isn't it? We never had any problems after this incident as products were checked only by using measuring meters.

